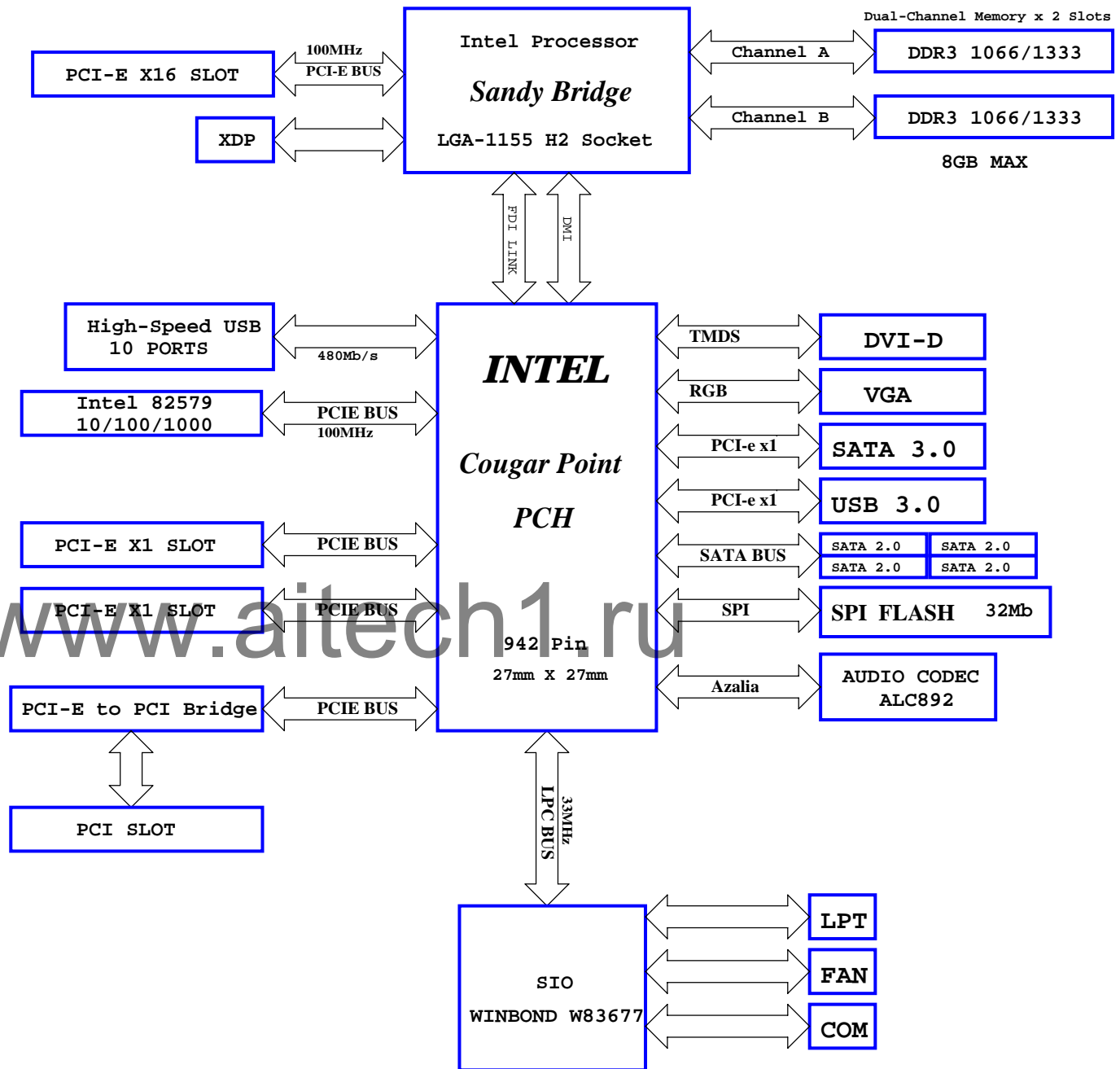


**IPM61-BE**  
Revision: 1.00

PAGE	TITLE
01	BLOCK DIAGRAM
02	CHANGE HISTORY - 1
03	CHANGE HISTORY - 2
04	CLOCKS DISTRIBUTION
05	SIGNAL & RESET MAP
06	POWER FLOW
07	POWER DISTRIBUTION
08	POWER SEQUENCE
09~14	INTEL CPU_SOCKET1155(1~6)
15	PLTRST_CPU# & RSMRST#
16~18	DDR3 & TERMINATION
19~27	INTEL_PCH(1~9)
28	PCH_DPWROK & SUS_ACK#
29	*****
30	VGA CONNECTOR
31	DVI-D CONNECTOR
32	PCI EXPRESS X16 SLOT
33	PCI SLOT
34	PCI EXPRESS X1 SLOT x2
35	INTEL 82579 LAN CONTROLLER
36	RJ45+USB2.0 CONNECTOR
37	PRINT PORT
38	SERIAL PORT
39	USB 3.0 CONTROLLER
40	USB 3.0 POWER
41~42	RJ45+USB 3.0 CONTROLLER
43~46	REALTEK ALC892 AUDIO CIRCUIT
47	PCI-E to PCI Bridge
48~49	USB HEADER
50	SATA CONN
51	SATA 3.0 CONTROLLER
52~53	SUPER I/O -WINBOND W83677
54	SMBUS CONTROL
55	TPM
56~57	FAN circuit
58	FRONT PANEL CIRCUIT
59	SPI ROM
60	ATX POWER_24P CONNECTOR
61	+3VA & +3VSB & +5VSB
62	+1P5V_DUAL
63	+VTT_DDR & +1P5V_DUAL_EN
64	+1P8V FOR SATA3.0 CONTROLLER
65	VSA_OV_Function
66	+0P925V_SA & +1P05V_PCH
67	5V DUAL POWER
68	+1P8V_SFR
69	+1V_USB3 & VRM_EN
70	+3P3V_LAN & +3P3V_ME
71~72	+1P05V_CPUIO
73~75	VCORE CONTROLLER + DRIVER
76	+V_AXG DRIVER
77	PS2 + USB CONN

78	EMI CAP
79	RTC/LED/SPKR/SCREW
80	BIOS and LPC header
81	Heceta Fan Control
82	CPU XDP DEBUG CONNECTOR
83	PCH XDP DEBUG CONNECTOR



**PEGATRON** Title : BLOCK DIAGRAM

Size	Project Name	Rev
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Date: Friday, September 21, 2018	Sheet: 1	of: 66
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## CAD Note:

Property: BOM

I = Installed Part.

NI = Not Installed Part.

PROTO = PROTO Phase Only.

VP = Virtual Part.

**<Version Name> REGATRON DT-MB RESTRICTED SECRET**

**PEGATRON** Title : CHANGE HISTORY-1

Pegatron Corp.

Engineer: *Livy\_Zhu*

Size

Size	Project Name
------	--------------

A3

**IPMSB-BE/CR**

Date: Friday, September 24, 2010

Sheet 2 of 83

1.00

## Schematics Change History

[illegible]

**CAD Note:**

Default component footprint is SMD 0402, Y5V, 5% type. Difference footprint show on schematics.

Property: BOM

I = Installed Part.

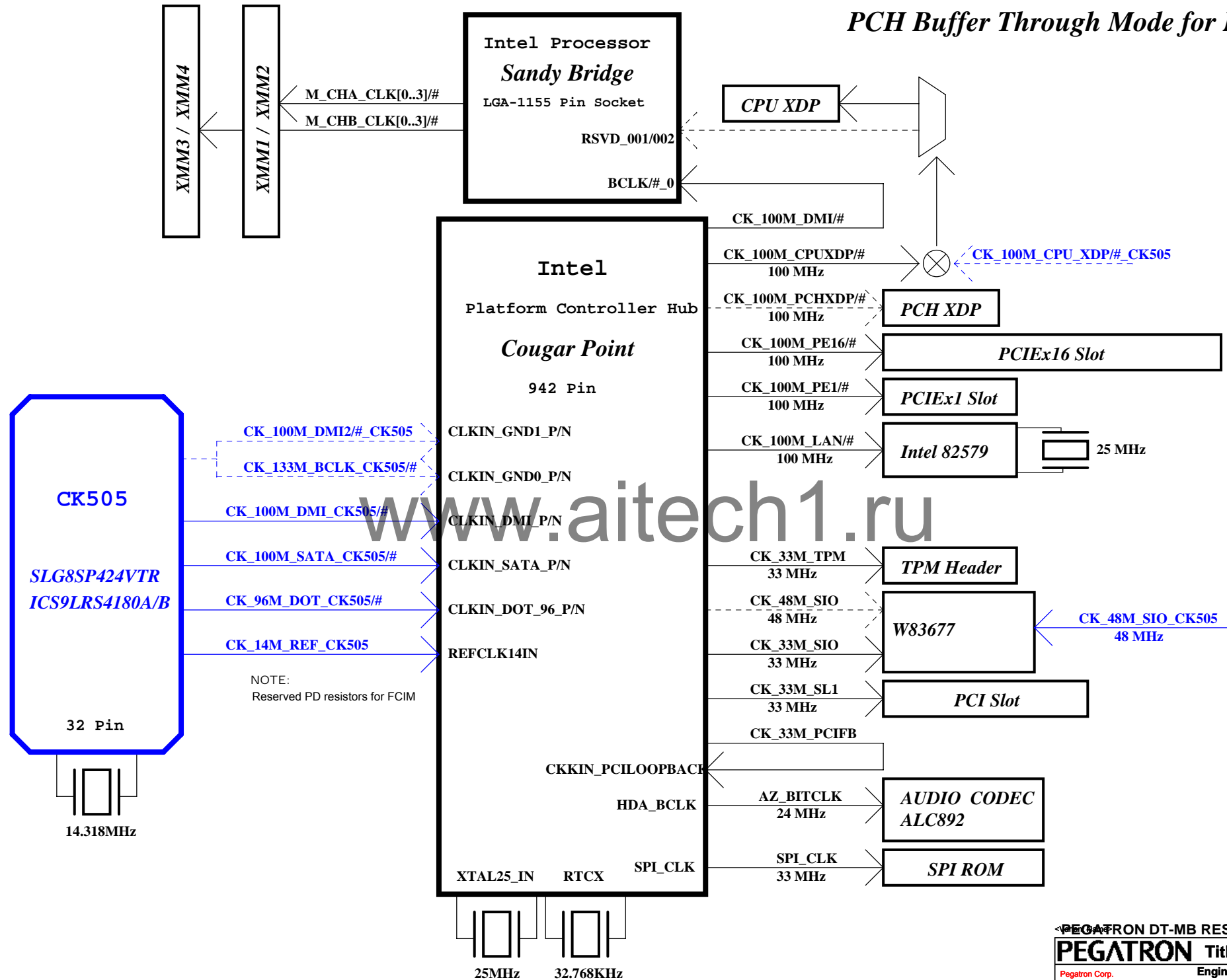
NI = Not Installed Part.

PROTO = PROTO Phase Only.

VP = Virtual Part.

<div style="text-align: center;"> <b>&lt;P&amp;CATRON DT-MB RESTRICTED SECRET</b>  <b>P&amp;CATRON</b>    Title : <b>CHANGE HISTORY-2</b> </div>			
<b>P&amp;catron Corp.</b>		<b>Engineer:</b> <i>Livy_Zhu</i>	
Size <b>A3</b>	Project Name <b>IPMSB-BE/CR</b>	Rev <b>1.00</b>	
Date: <b>Friday, September 24, 2010</b>	Sheet <b>3</b> of <b>83</b>		

## *PCH Buffer Through Mode for Pre-Silicon*



**<Version Name> PEGATRON DT-MB RESTRICTED SECRET**

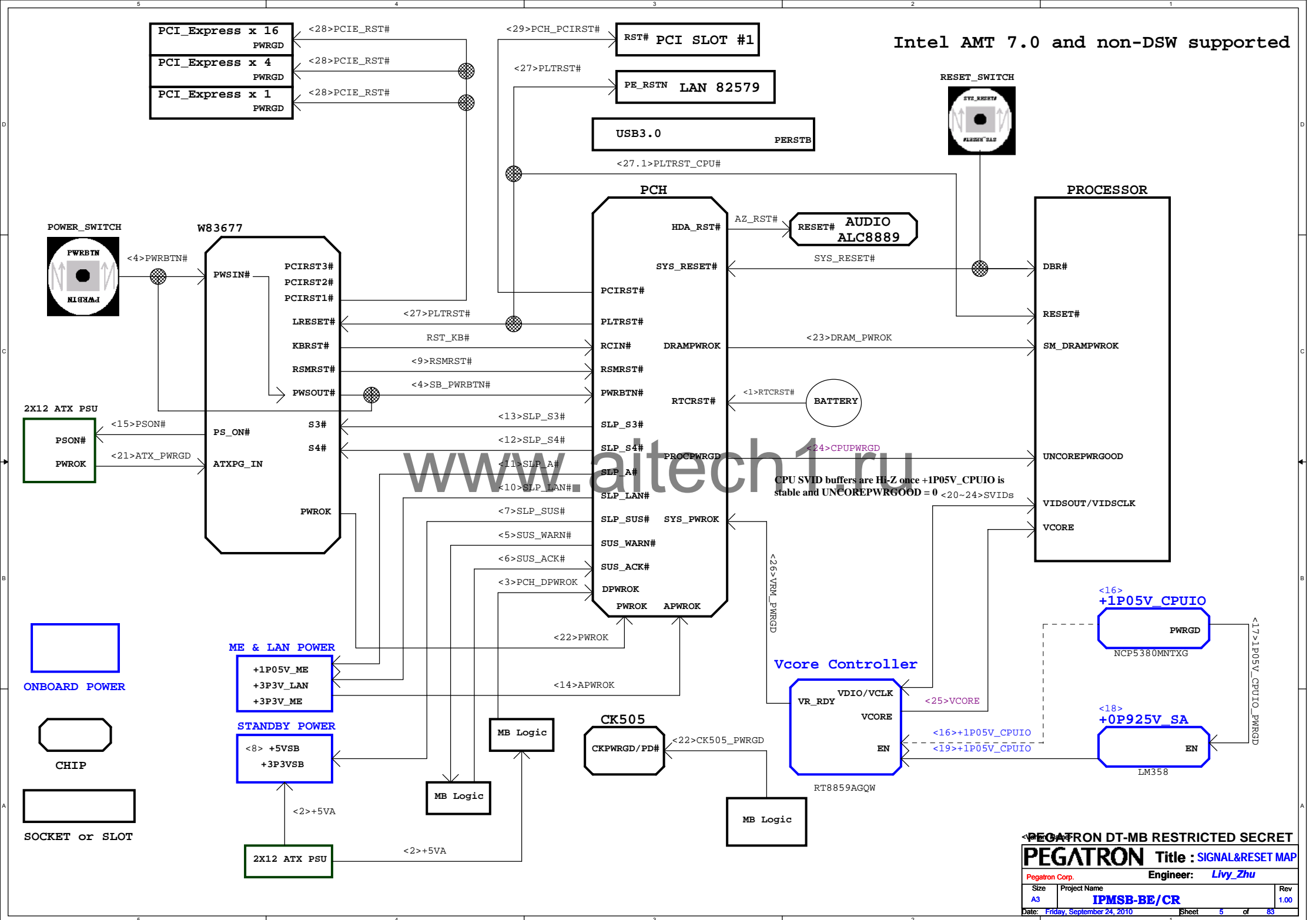
**PEGATRON** Title : CLCOK DISTRIBUTION

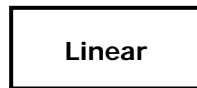
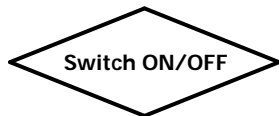
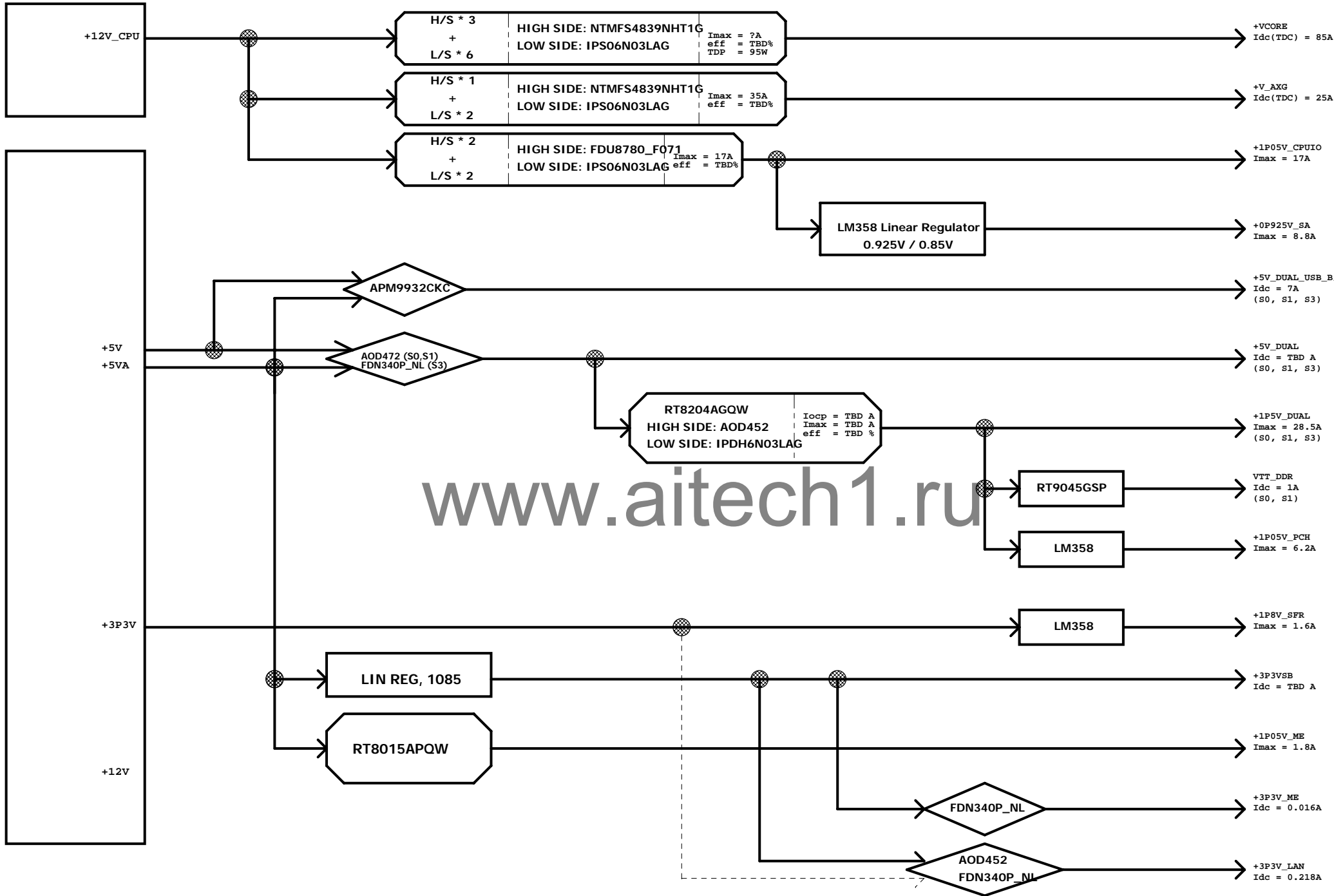
Pegatron Corp. Engineer: *Livy\_Zhu*

Size <b>A3</b>	Project Name <b>IPMSB-BE/CR</b>	Rev <b>1.00</b>
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Date: Friday, September 24, 2010 Sheet 4 of 83

Intel AMT 7.0 and non-DSW supported





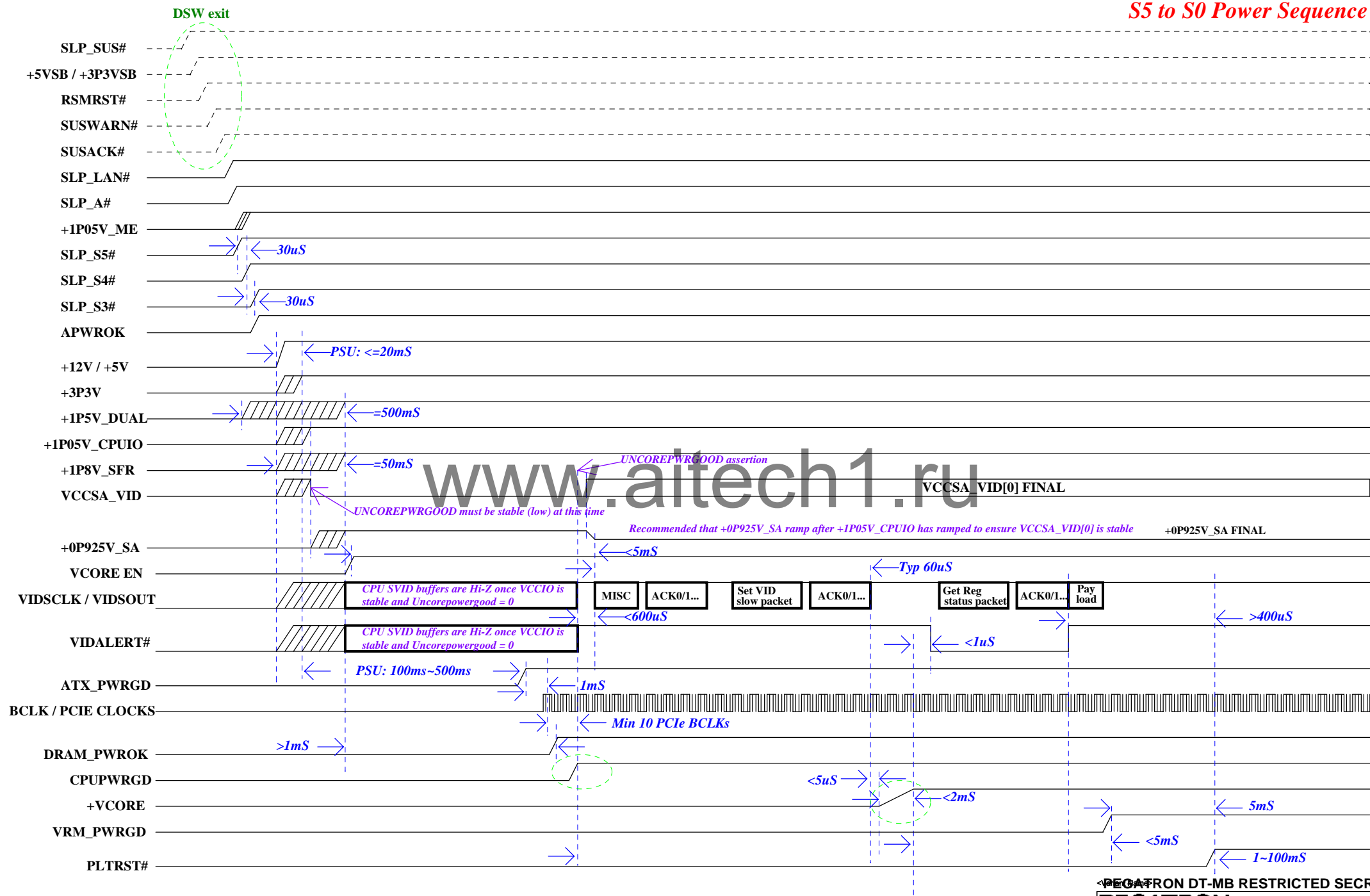
Note: lxx/loo means  
ltdc/lmax

	<b>CPU Sandy Bridge</b>
+VCORE	-> 95A(TDC) - 95W
+1P05V_CPUIO	-> 17A(I <sub>max</sub> ) - W
+0P925V_SA	-> 8.8A(I <sub>max</sub> ) - W
+V_AXG	-> 25A(TDC) - W
	<b>CLOCK GEN</b>
+3P3V	-> 125mA - W
	<b>PCH</b>
+1P05V_PCH	-> 5.831A - W
+1P05V_CPUIO	-> 0.043A - W
+1P8V_SFR	-> 0.16A - W
+3P3V	-> 0.267A - W
+3P3VSB	-> 0.107A - W
+1P05V_ME	-> 1.01A - W
+3P3V_ME	-> 0.02A - W
+3P3VA	-> 0.002A - W
+BATT	RTC(G3) -> 6uA - 0.0198mW
	<b>DDR2 DIMM (4) &amp; Termination</b>
+1P5V_DUAL	VDD (S0, S1, S3) ->7.5 A - 11.25W
+VTT_DDR(0.75V)	SM VTT (S0, S1) -> 1A - 0.75W

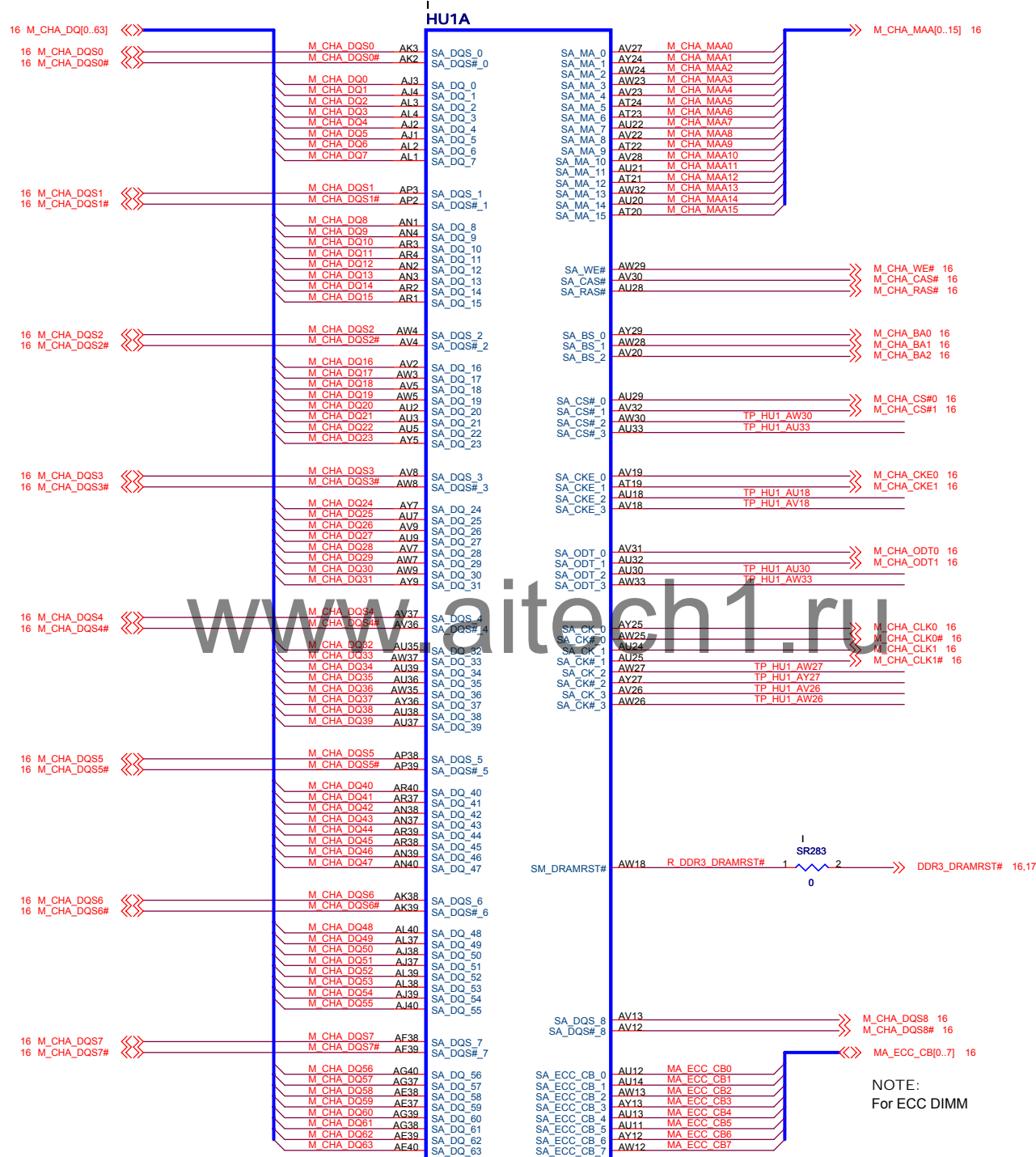
	<b>PCI Express x 1</b>
+12V	-> 5A - 60W
+3P3V	-> 3.0A - 9.9W
+3P3VSB	WAKE -> 0.375A - 1.24W No WAKE-> 20mA - 66mW
	<b>PCI Express x 16</b>
+12V	-> 5.5A - 66W
+3P3V	-> 3.0A - 9.9W
+3P3VSB	WAKE -> 0.375A - 1.24W No WAKE-> 20mA - 66mW
	<b>PCI SLOTS</b>
+12V	-> 0.5A - 6W
-12V	-> 0.1A - 1.2W
+5V	-> 5.0A - 25W
+3P3V	-> 7.6A - 25.08W
+3P3VSB	WAKE -> 0.375A - 1.24W No WAKE-> 20mA - 66mW
	<b>INTEL 82579</b>
+3P3V_LAN	-> mA - 720mW
	<b>83677</b>
+3P3V	-> 35mA - mW
	<b>ALC892</b>
+3P3V	-> mA - mW

	<b>FL1009 USB3.0</b>
+3P3V	-> mA - W
+1P05V_USB	-> mA - W
	<b>USB 14 PORTS</b>
+5V_DUAL_B/F	(S0, S1) -> 7A - 35W
	<b>DVI</b>
+5V	-> mA - mW
	-> mA - mW
	<b>FANS</b>
+12V	-> 1.2A - 14.4W
	<b>PS2 KB/MS</b>
+5V_DUAL	(S0, S1) -> 0.345A - 1.73W (S3) -> 2mA - 10mW
	<b>SP1</b>
+3P3V_ME	-> 30mA - 99mW

# S5 to S0 Power Sequence



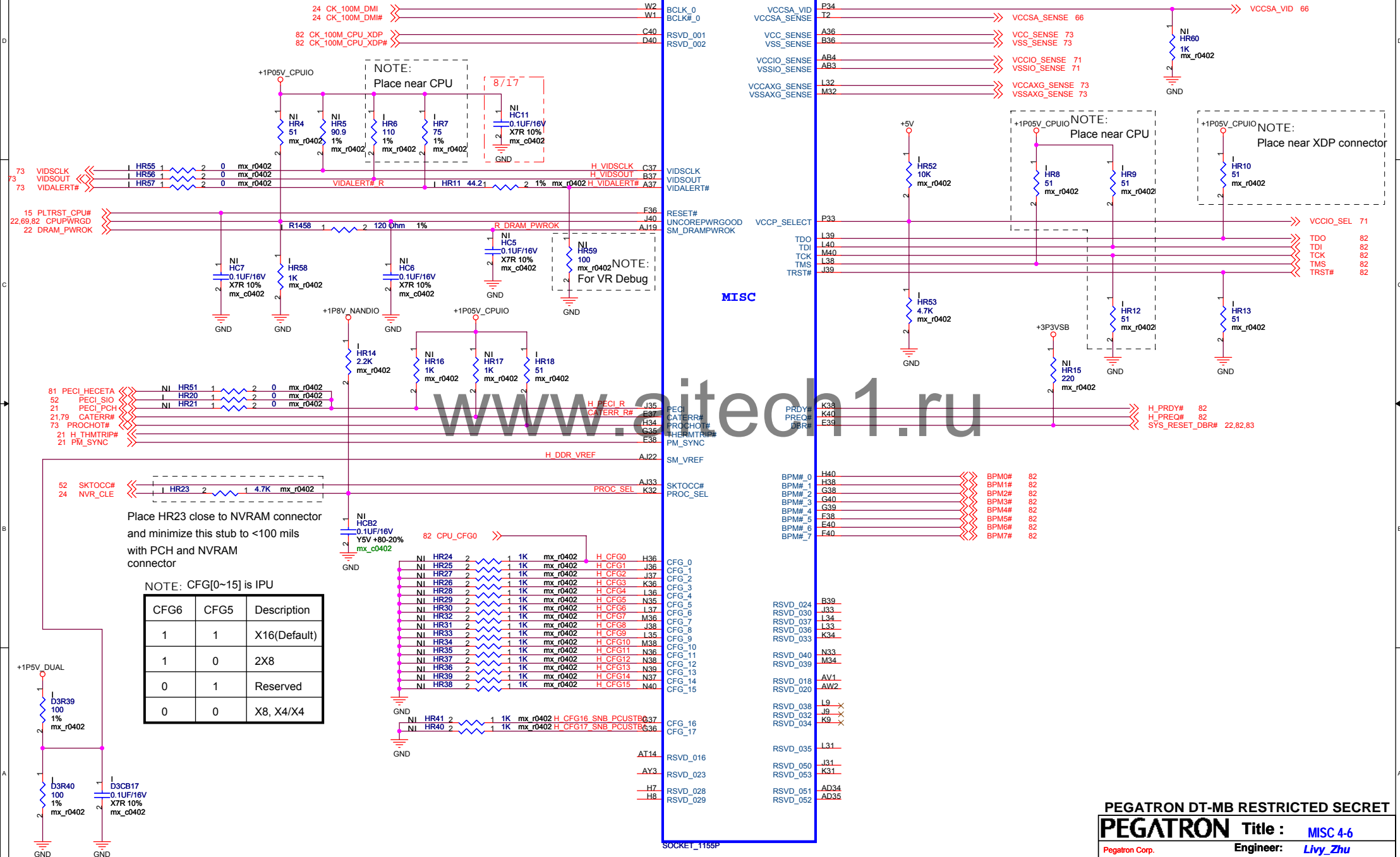








# HU1E



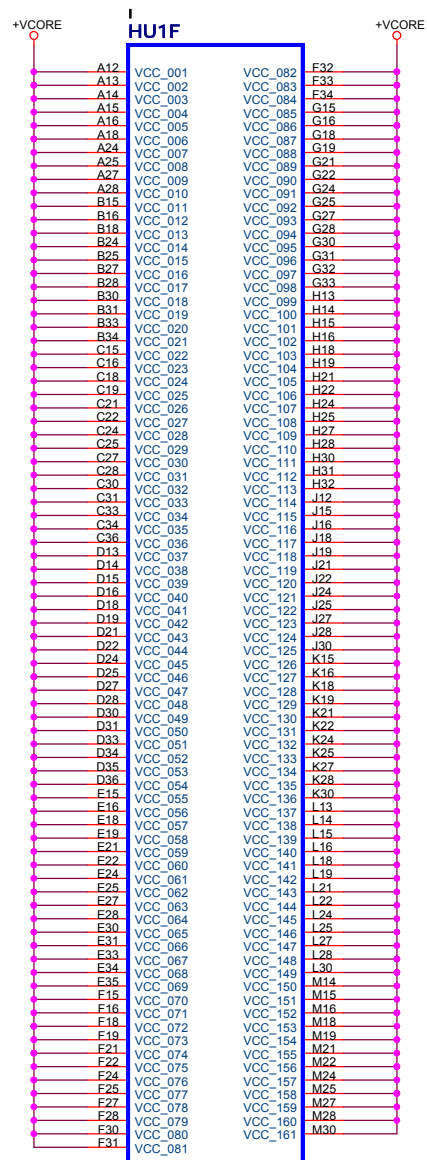
PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title : **MISC 4-6**

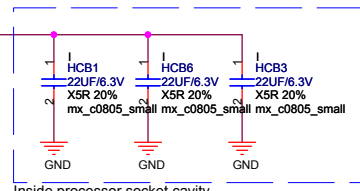
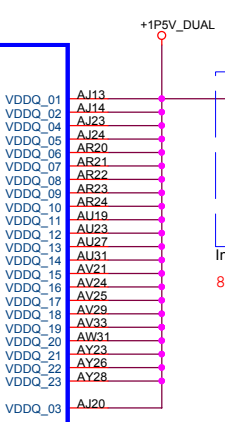
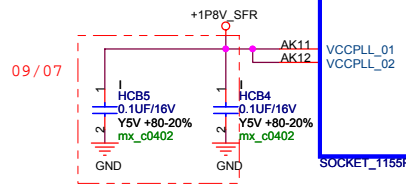
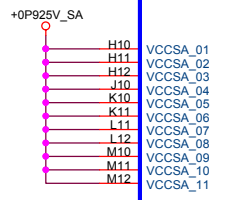
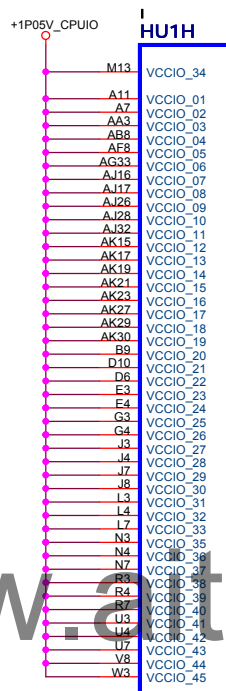
Pegatron Corp. Engineer: **Livy Zhu**

Size **A3** Project Name **IPMSB-BE/CR** Rev **1.00**

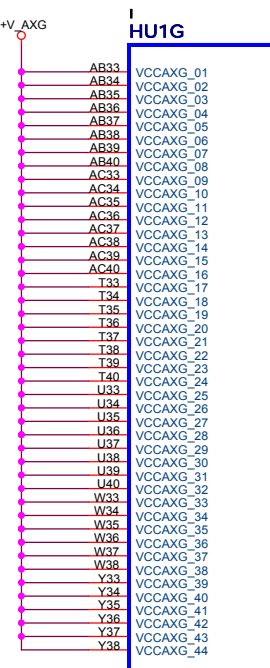
Date: **Friday, September 24, 2010** Sheet **12** of **83**



SOCKET\_1155P



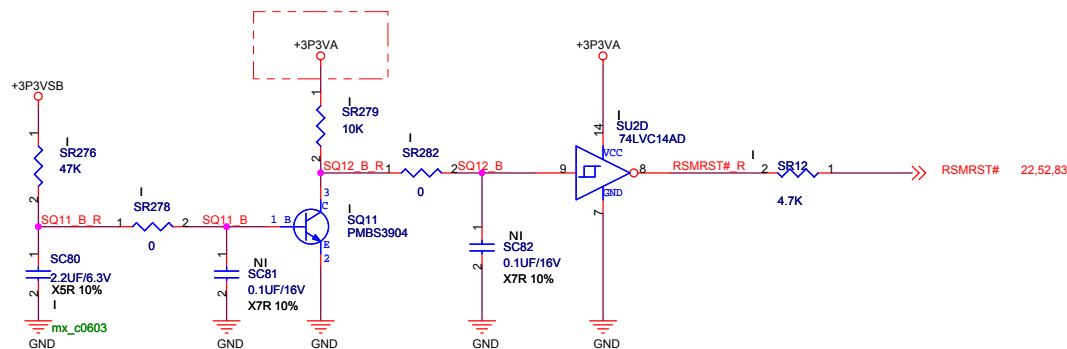
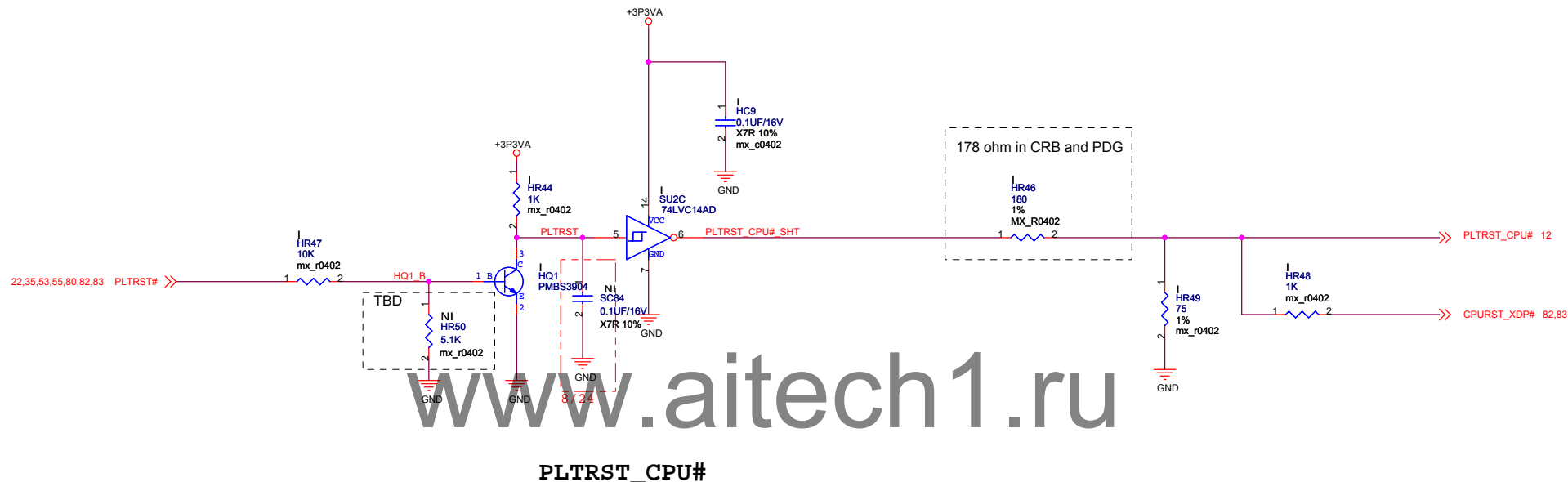
Inside processor socket cavity  
8/17: change to 22UF 11X234226160



SOCKET\_1155P

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PEGATRON DT-MB RESTRICTED SECRET

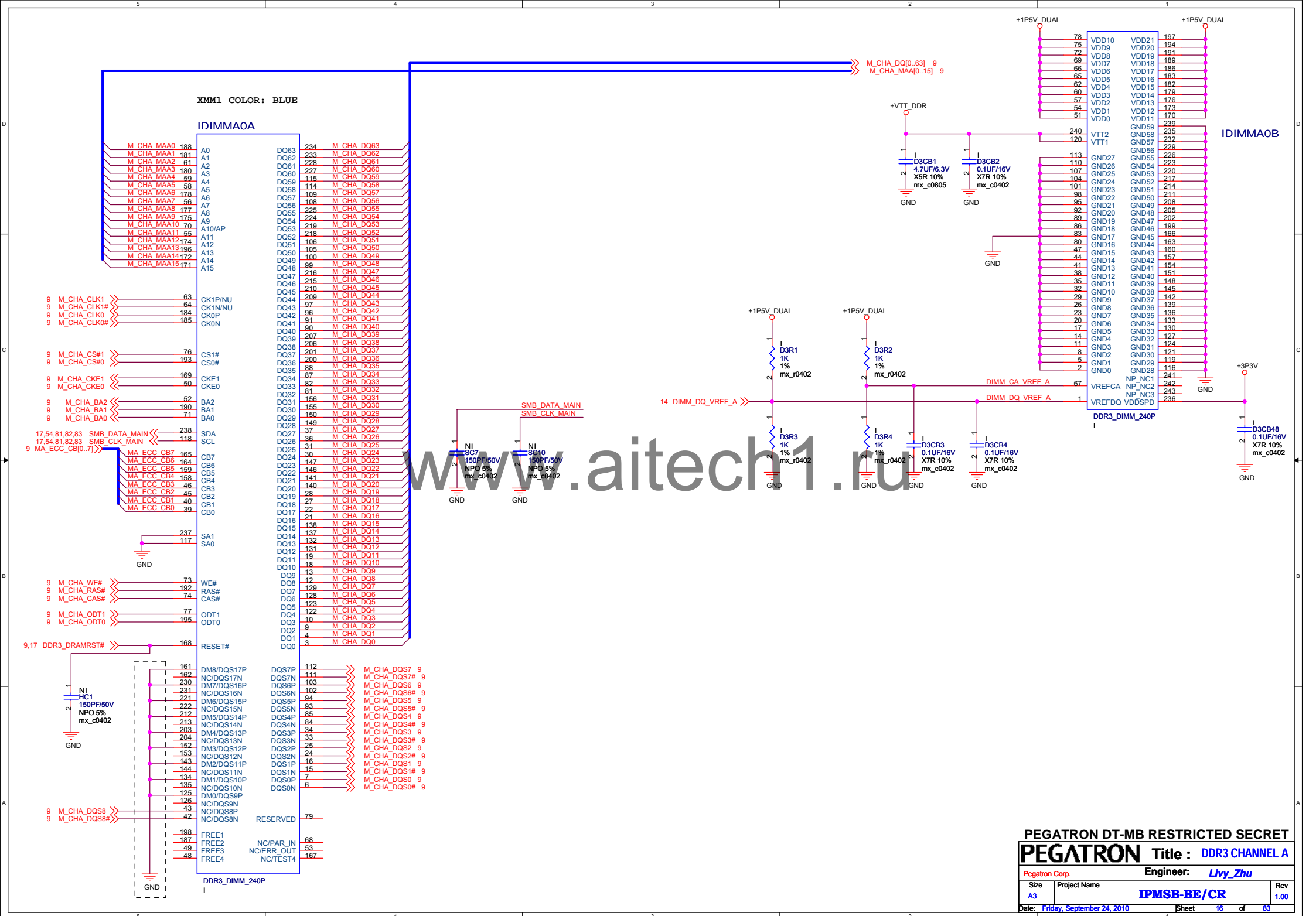
**PEGATRON** Title : PLTRST\_CPU#

Pegatron Corp. Engineer: Livy\_Zhu

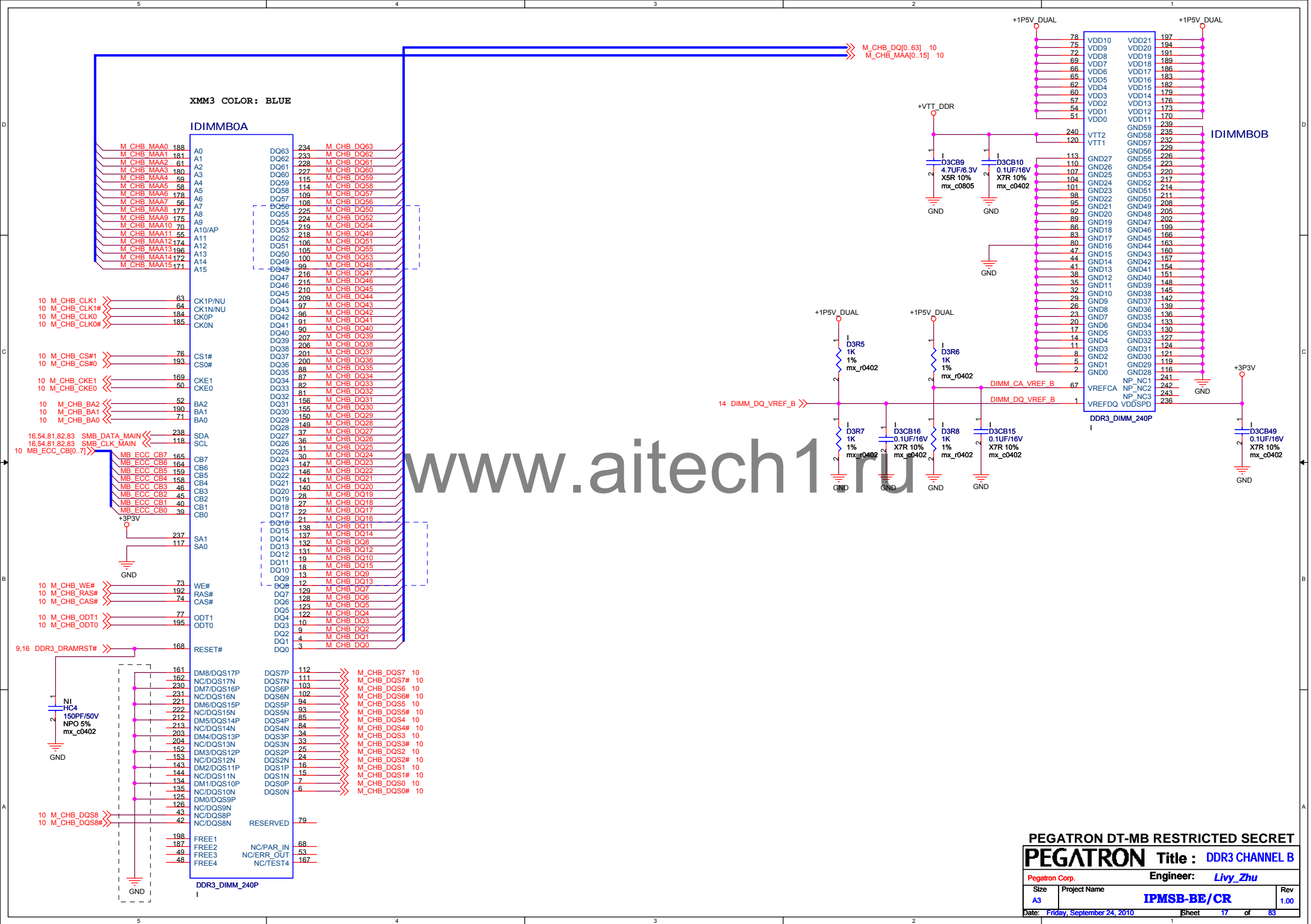
Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

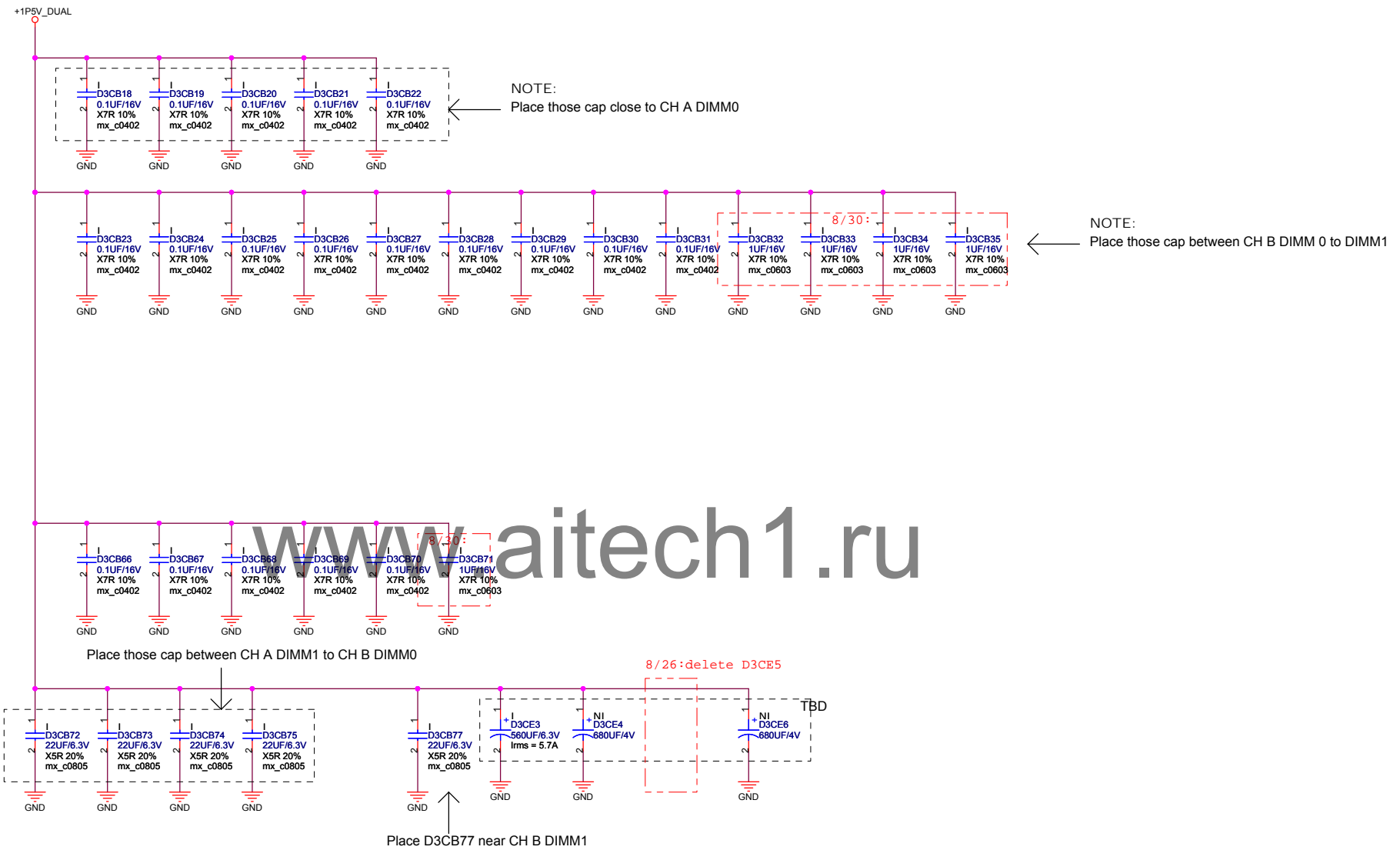
Date: Friday, September 24, 2010 Sheet 15 of 83

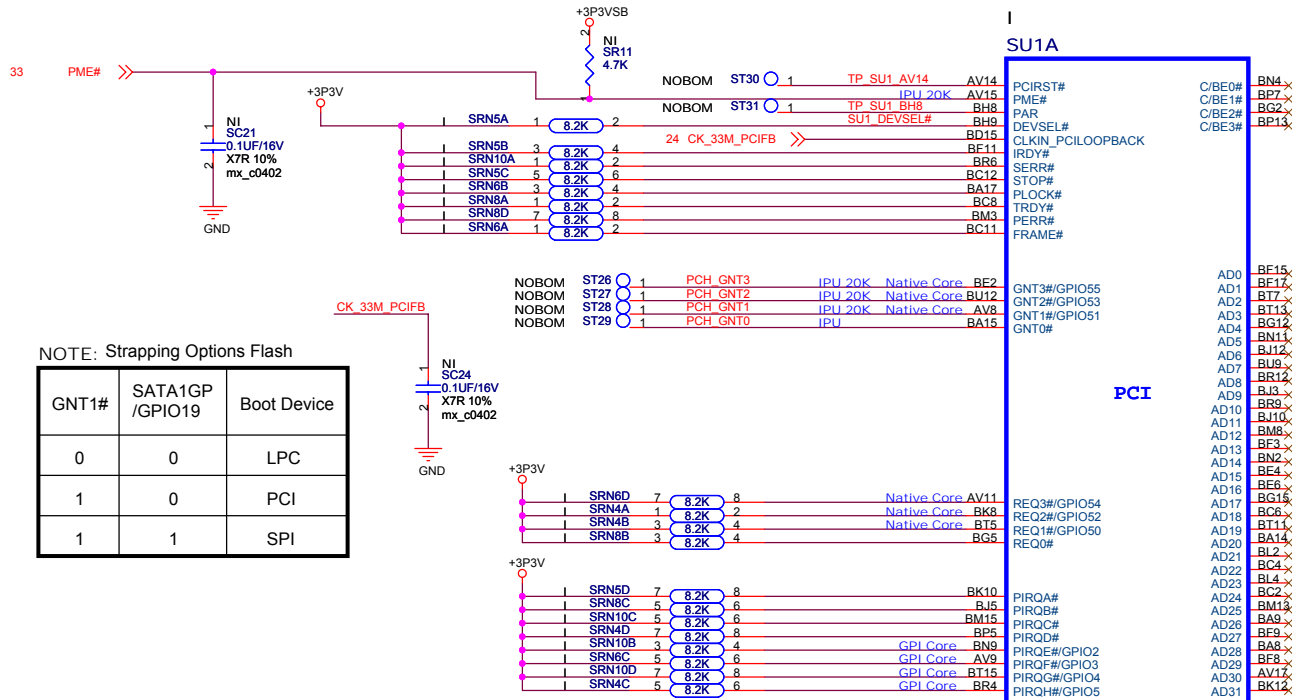






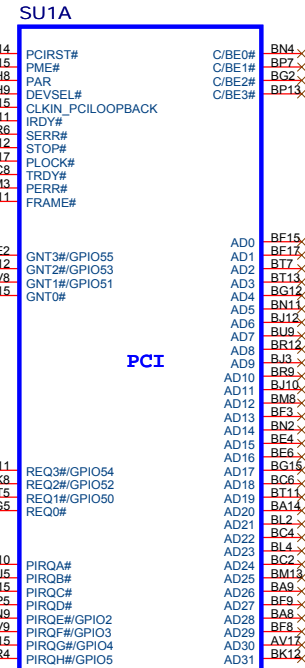
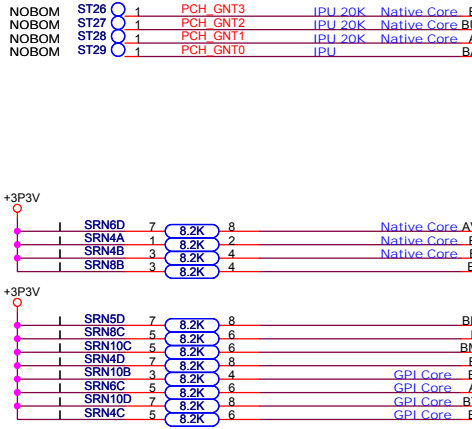






NOTE: Strapping Options Flash

GNT1#	SATA1GP /GPIO19	Boot Device
0	0	LPC
1	0	PCI
1	1	SPI



PCI

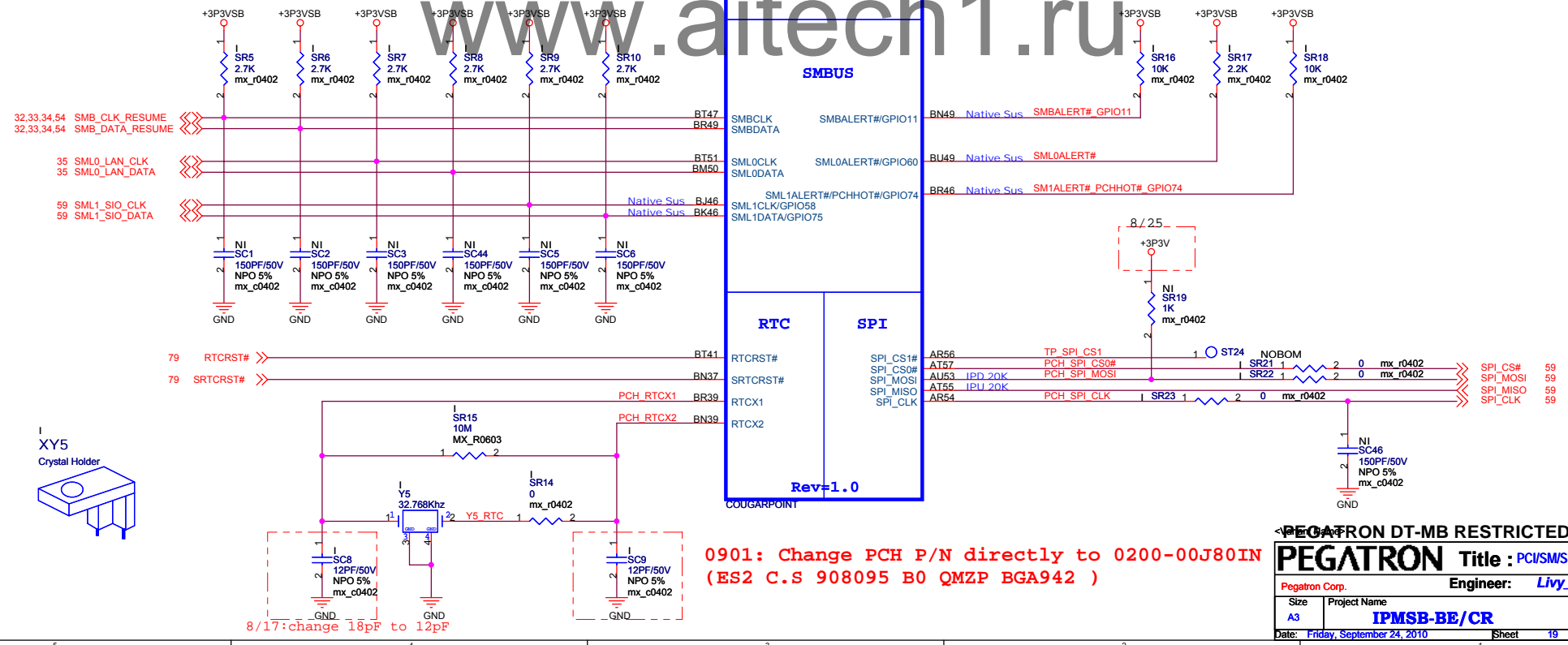
SMBUS

RTC

SPI

Rev=1.0

COUGARPOINT



0901: Change PCH P/N directly to 0200-00J80IN (ES2 C.S 908095 B0 QMZF BGA942 )

PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title : PC/SM/SPI/RTC-1.9

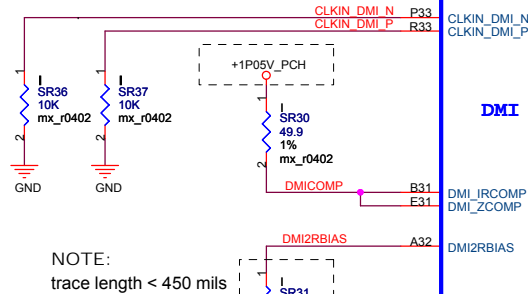
Pegatron Corp. Engineer: *Livy\_Zhu*

Size A3	Project Name IPMSB-BE/CR	Rev 1.00
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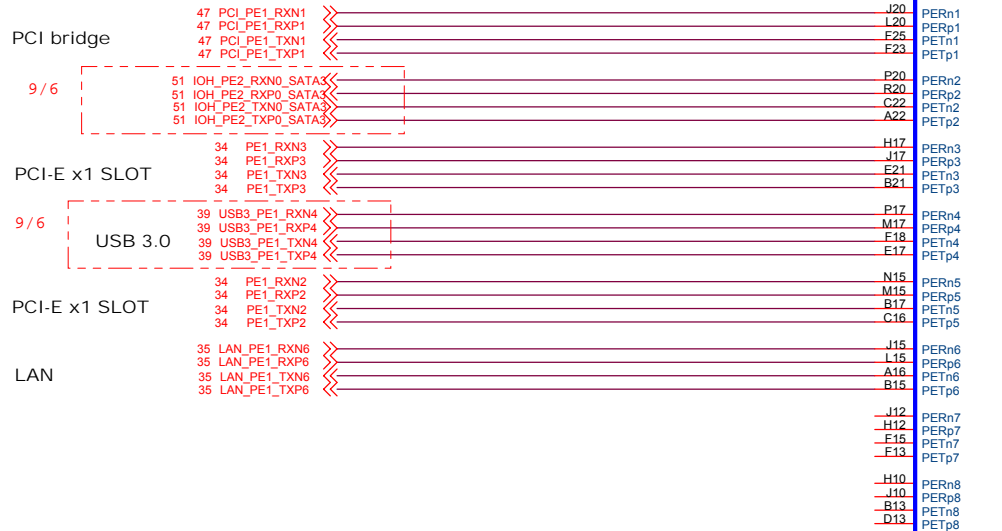
Date: Friday, September 24, 2010 Sheet 19 of 83

USB ports 6,7,12,13 are disabled for H61

NOTE:  
Used for for DMI, PCIe(Pcie 2.0 jitter spec compliant).

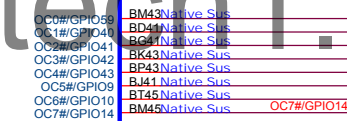


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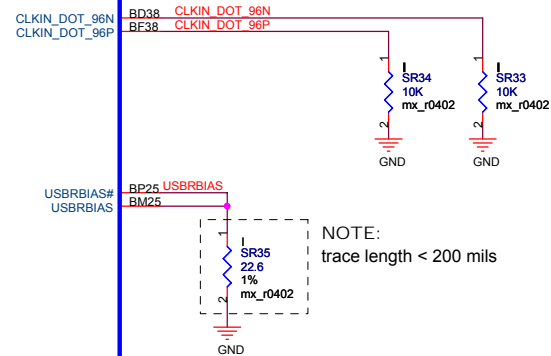


USB

PCI-E



NOTE:  
Used for integrated graphics, generate USB backbone,  
24MHz HDA bit, and 48MHz clock.



Front USB Header

PS2+USB

For BE: Front USB Header  
For CR: LAN+USB

PEGATRON DT-MB RESTRICTED SECRET

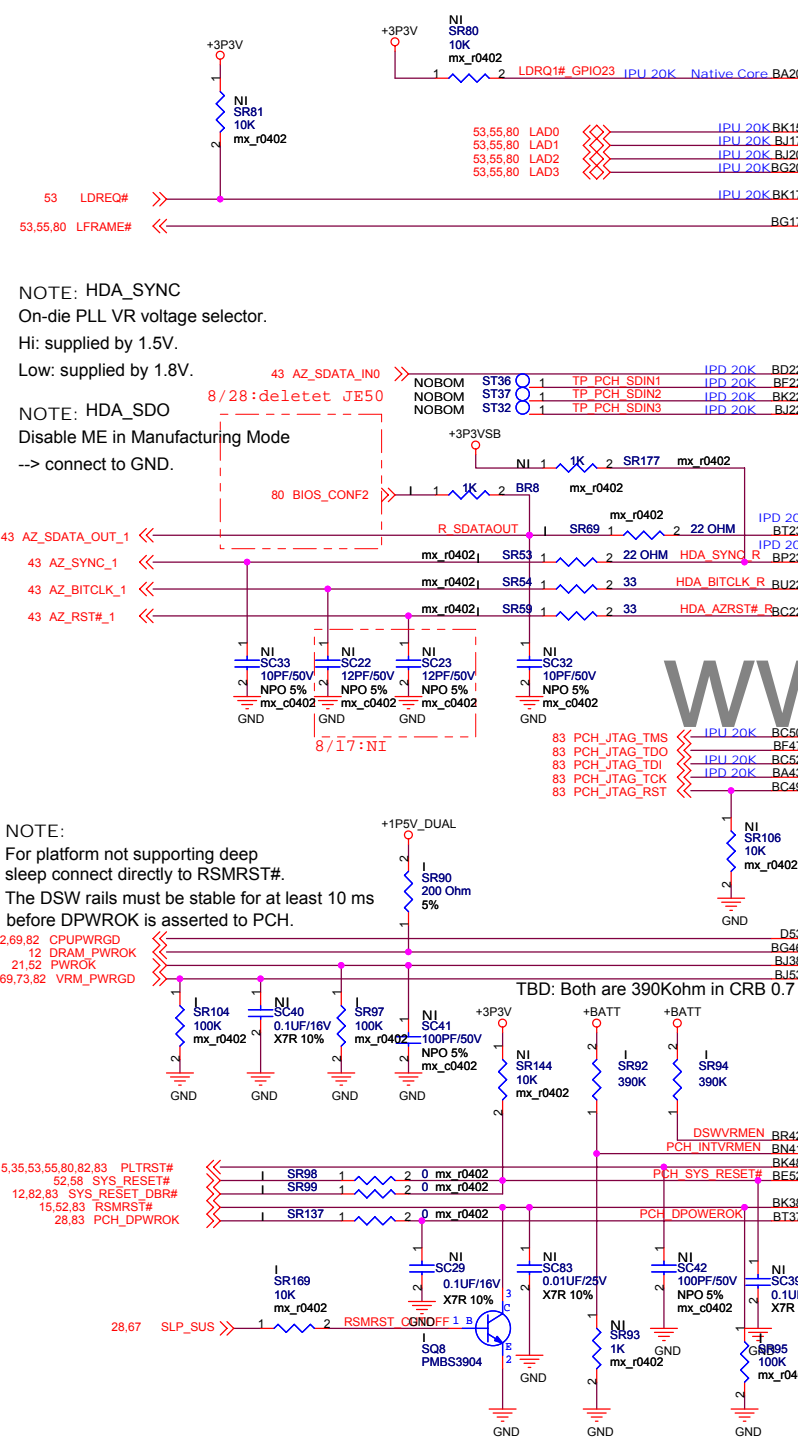
PEGATRON Title : PCIE/USB/DMI 2-9

Pegatron Corp. Engineer: Livy\_Zhu

Size A3 Project Name IPMSB-BE/CR

Date: Friday, September 24, 2010 Sheet 20 of 83

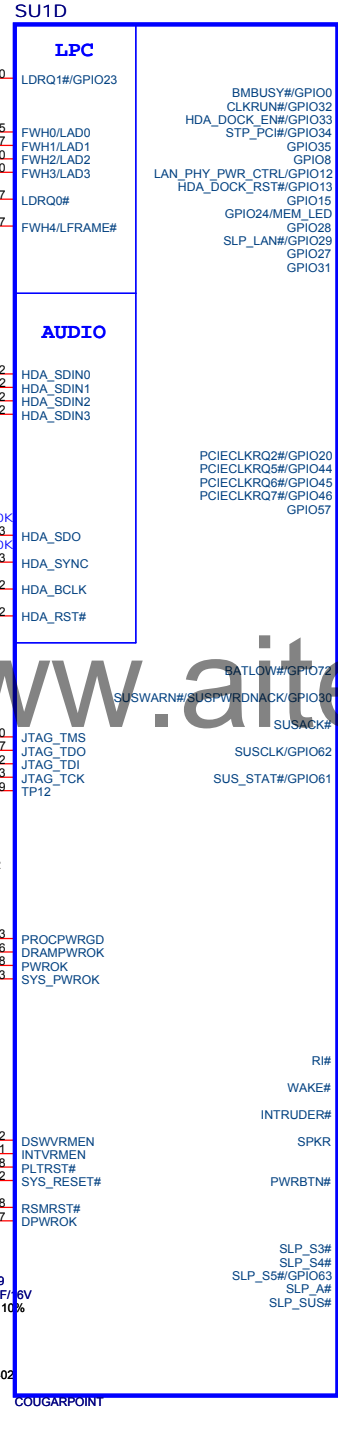




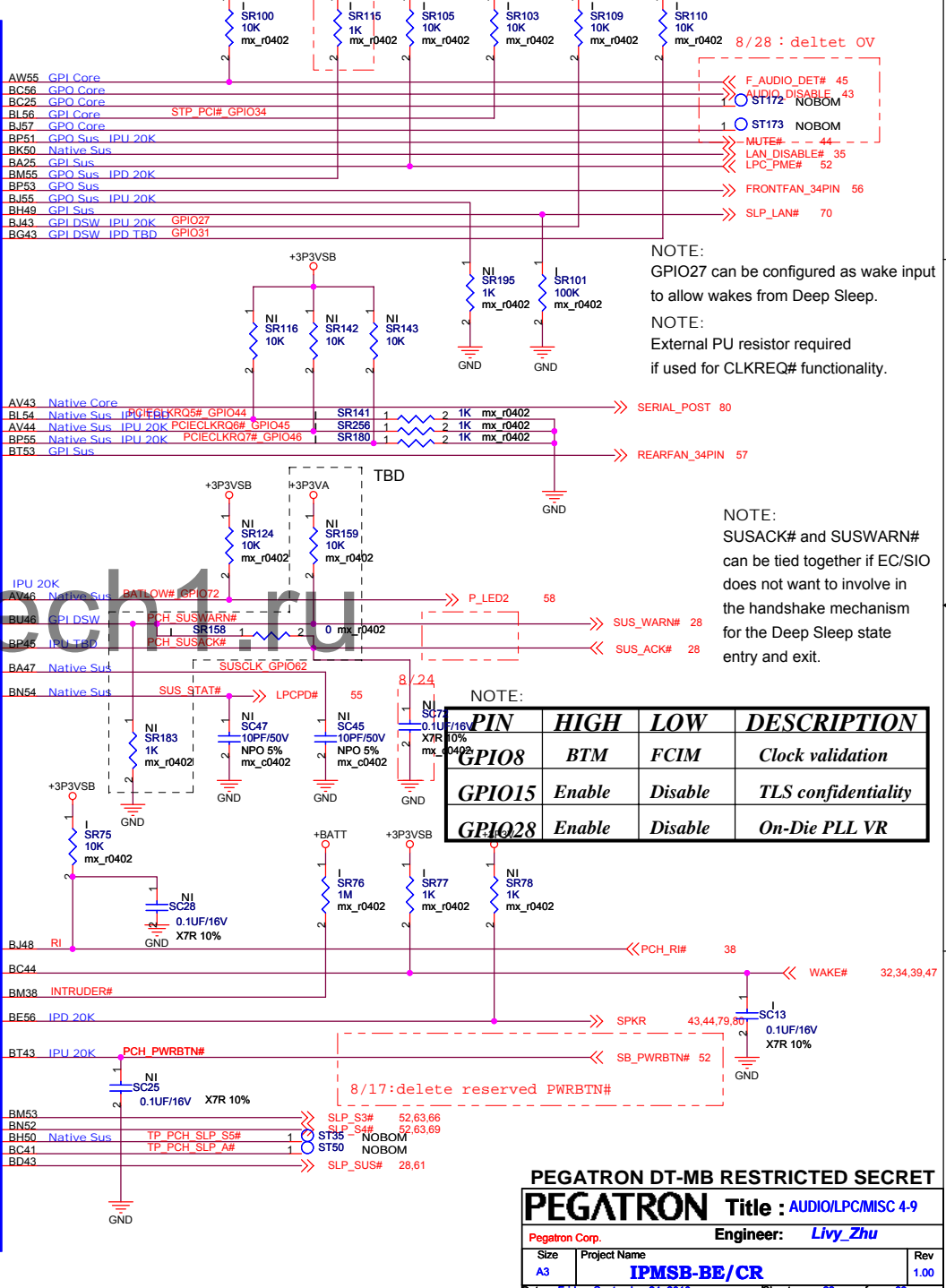
NOTE: HDA\_SYNC  
On-die PLL VR voltage selector.  
Hi: supplied by 1.5V.  
Low: supplied by 1.8V.

NOTE: HDA\_SDO  
Disable ME in Manufacturing Mode  
--> connect to GND.

NOTE:  
For platform not supporting deep sleep connect directly to RSMRST#.  
The DSW rails must be stable for at least 10 ms before DPWROK is asserted to PCH.



COUGARPOINT



PIN	HIGH	LOW	DESCRIPTION
GPIO8	BTM	FCIM	Clock validation
GPIO15	Enable	Disable	TLS confidentiality
GPIO28	Enable	Disable	On-Die PLL VR

## SU1E

Y18  
Y17  
AB18  
AB17

TP6  
TP7  
TP8  
TP9

30 VGA\_DDCA\_CLK  
30 VGA\_DDCA\_DATA

AW3  
AW1

CRT\_DDC\_CLK  
CRT\_DDC\_DATA

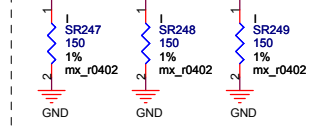
CRT\_HSYNC  
CART\_VSYNC  
CART\_RED  
CART\_GREEN  
CART\_BLUE

AR4  
AR2  
AN6  
AN2  
AM1

VGA\_HSYNC 3P3V  
VGA\_VSYNC 3P3V  
VGA\_RED S  
VGA\_GREEN S  
VGA\_BLUE S

SR245 1 2 33 mx\_r0402  
SR246 1 2 33 mx\_r0402  
JP20 1 2 SHORT\_PIN NOBOM  
JP21 1 2 SHORT\_PIN NOBOM  
JP22 1 2 SHORT\_PIN NOBOM

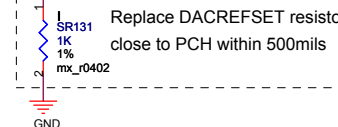
NOTE:  
Place RGB resistors close to PCH within 250mils



DAC\_IREF  
CRT\_IRTN

AT3  
AM6

DACREFSET



Replace DACREFSET resistor  
close to PCH within 500mils

DDPB\_0P  
DDPB\_0N  
DDPB\_1P  
DDPB\_1N  
DDPB\_2P  
DDPB\_2N  
DDPB\_3P  
DDPB\_3N

R14  
R12  
M11  
M12  
H8  
K8  
L5  
M3

DVI\_TMDSB\_DATA0# 31  
DVI\_TMDSB\_DATA0# 31  
DVI\_TMDSB\_DATA1# 31  
DVI\_TMDSB\_DATA1# 31  
DVI\_TMDSB\_DATA2# 31  
DVI\_TMDSB\_DATA2# 31  
DVI\_TMDSB\_CLK# 31  
DVI\_TMDSB\_CLK# 31

DVI

SDVO\_INTP  
SDVO\_INTN  
SDVO\_STALLP  
SDVO\_STALLN  
SDVO\_TVCLKINP  
SDVO\_TVCLKINN

U2  
T3  
W3  
U5  
U8  
U9

IPD 50  
IPD 50  
IPD 50  
IPD 50  
IPD 50  
IPD 50

ST78 NOBOM  
ST79 NOBOM  
ST78 NOBOM  
ST79 NOBOM  
ST78 NOBOM  
ST79 NOBOM

NOBOM ST84  
NOBOM ST83

TP\_PCH DDPDAUXP  
TP\_PCH DDPDAUXN

U14  
U12

DDPC\_AUXP  
DDPC\_AUXN

DDPC\_0P  
DDPC\_0N  
DDPC\_1P  
DDPC\_1N  
DDPC\_2P  
DDPC\_2N  
DDPC\_3P  
DDPC\_3N

TP\_PCH L2  
TP\_PCH J3  
TP\_PCH G2  
TP\_PCH G4  
TP\_PCH F3  
TP\_PCH F5  
TP\_PCH E4  
TP\_PCH E2

ST90 NOBOM  
ST93 NOBOM  
ST94 NOBOM  
ST102 NOBOM  
ST103 NOBOM  
ST104 NOBOM  
ST130 NOBOM  
ST139 NOBOM

DDPC\_CTRLCLK  
DDPC\_CTRLDATA

DDPC\_0P  
DDPC\_0N  
DDPC\_1P  
DDPC\_1N  
DDPC\_2P  
DDPC\_2N  
DDPC\_3P  
DDPC\_3N

TP\_PCH D5  
TP\_PCH B5  
TP\_PCH C6  
TP\_PCH D7  
TP\_PCH B7  
TP\_PCH C9  
TP\_PCH E11  
TP\_PCH B11

ST146 NOBOM  
ST147 NOBOM  
ST141 NOBOM  
ST140 NOBOM  
ST143 NOBOM  
ST142 NOBOM  
ST145 NOBOM  
ST144 NOBOM

DDPD\_AUXP  
DDPD\_AUXN  
DDPD\_CTRLCLK  
DDPD\_CTRLDATA

DDPD\_0P  
DDPD\_0N  
DDPD\_1P  
DDPD\_1N  
DDPD\_2P  
DDPD\_2N  
DDPD\_3P  
DDPD\_3N

TP\_PCH D5  
TP\_PCH B5  
TP\_PCH C6  
TP\_PCH D7  
TP\_PCH B7  
TP\_PCH C9  
TP\_PCH E11  
TP\_PCH B11

ST146 NOBOM  
ST147 NOBOM  
ST141 NOBOM  
ST140 NOBOM  
ST143 NOBOM  
ST142 NOBOM  
ST145 NOBOM  
ST144 NOBOM

DDPD\_AUXP  
DDPD\_AUXN  
DDPD\_CTRLCLK  
DDPD\_CTRLDATA

DDPD\_0P  
DDPD\_0N  
DDPD\_1P  
DDPD\_1N  
DDPD\_2P  
DDPD\_2N  
DDPD\_3P  
DDPD\_3N

TP\_PCH D5  
TP\_PCH B5  
TP\_PCH C6  
TP\_PCH D7  
TP\_PCH B7  
TP\_PCH C9  
TP\_PCH E11  
TP\_PCH B11

ST146 NOBOM  
ST147 NOBOM  
ST141 NOBOM  
ST140 NOBOM  
ST143 NOBOM  
ST142 NOBOM  
ST145 NOBOM  
ST144 NOBOM

DDPD\_AUXP  
DDPD\_AUXN  
DDPD\_CTRLCLK  
DDPD\_CTRLDATA

DDPD\_0P  
DDPD\_0N  
DDPD\_1P  
DDPD\_1N  
DDPD\_2P  
DDPD\_2N  
DDPD\_3P  
DDPD\_3N

TP\_PCH D5  
TP\_PCH B5  
TP\_PCH C6  
TP\_PCH D7  
TP\_PCH B7  
TP\_PCH C9  
TP\_PCH E11  
TP\_PCH B11

ST146 NOBOM  
ST147 NOBOM  
ST141 NOBOM  
ST140 NOBOM  
ST143 NOBOM  
ST142 NOBOM  
ST145 NOBOM  
ST144 NOBOM

DDPD\_AUXP  
DDPD\_AUXN  
DDPD\_CTRLCLK  
DDPD\_CTRLDATA

DDPD\_0P  
DDPD\_0N  
DDPD\_1P  
DDPD\_1N  
DDPD\_2P  
DDPD\_2N  
DDPD\_3P  
DDPD\_3N

TP\_PCH D5  
TP\_PCH B5  
TP\_PCH C6  
TP\_PCH D7  
TP\_PCH B7  
TP\_PCH C9  
TP\_PCH E11  
TP\_PCH B11

ST146 NOBOM  
ST147 NOBOM  
ST141 NOBOM  
ST140 NOBOM  
ST143 NOBOM  
ST142 NOBOM  
ST145 NOBOM  
ST144 NOBOM

DDPD\_AUXP  
DDPD\_AUXN  
DDPD\_CTRLCLK  
DDPD\_CTRLDATA

DDPD\_0P  
DDPD\_0N  
DDPD\_1P  
DDPD\_1N  
DDPD\_2P  
DDPD\_2N  
DDPD\_3P  
DDPD\_3N

TP\_PCH D5  
TP\_PCH B5  
TP\_PCH C6  
TP\_PCH D7  
TP\_PCH B7  
TP\_PCH C9  
TP\_PCH E11  
TP\_PCH B11

ST146 NOBOM  
ST147 NOBOM  
ST141 NOBOM  
ST140 NOBOM  
ST143 NOBOM  
ST142 NOBOM  
ST145 NOBOM  
ST144 NOBOM

DDPD\_AUXP  
DDPD\_AUXN  
DDPD\_CTRLCLK  
DDPD\_CTRLDATA

DDPD\_0P  
DDPD\_0N  
DDPD\_1P  
DDPD\_1N  
DDPD\_2P  
DDPD\_2N  
DDPD\_3P  
DDPD\_3N

TP\_PCH D5  
TP\_PCH B5  
TP\_PCH C6  
TP\_PCH D7  
TP\_PCH B7  
TP\_PCH C9  
TP\_PCH E11  
TP\_PCH B11

ST146 NOBOM  
ST147 NOBOM  
ST141 NOBOM  
ST140 NOBOM  
ST143 NOBOM  
ST142 NOBOM  
ST145 NOBOM  
ST144 NOBOM

DDPD\_AUXP  
DDPD\_AUXN  
DDPD\_CTRLCLK  
DDPD\_CTRLDATA

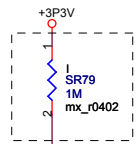
DDPD\_0P  
DDPD\_0N  
DDPD\_1P  
DDPD\_1N  
DDPD\_2P  
DDPD\_2N  
DDPD\_3P  
DDPD\_3N

TP\_PCH D5  
TP\_PCH B5  
TP\_PCH C6  
TP\_PCH D7  
TP\_PCH B7  
TP\_PCH C9  
TP\_PCH E11  
TP\_PCH B11

ST146 NOBOM  
ST147 NOBOM  
ST141 NOBOM  
ST140 NOBOM  
ST143 NOBOM  
ST142 NOBOM  
ST145 NOBOM  
ST144 NOBOM

NOTE:

DDP[B..D]\_HPD are 3.3V tolerant.



CRB 0.7 do not implement.

31 DDPB\_HPDI

NOBOM ST72  
NOBOM ST73

TP\_PCH DDPBAUXP  
TP\_PCH DDPBAUXN

R8  
R9

DDPB\_AUXP  
DDPB\_AUXN

SDVO\_CTRLCLK  
SDVO\_CTRLDATA

IPD 20K

AL15  
AL17

DDPB\_HPDI

NI  
SR120  
1K  
mx\_r0402

GND

DDPB\_HPDI

DDPB\_HPDI

DDPB\_HPDI

DDPB\_HPDI

DDPB\_HPDI

DDPB\_HPDI

DDPB\_HPDI

DDPB\_HPDI

DDPB\_HPDI

DDPB\_HPDI

DDPB\_HPDI

DDPB\_HPDI

DDPB\_HPDI

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DDPB\_HPDI

DDPB\_HPDI

DDPB\_HPDI

DDPB\_HPDI

COUGARPOINT

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : VGA/DP/HDMI 5-9

Pegatron Corp. Engineer: Livy\_Zhu

Size A3 Project Name IPMSB-BE/CR Rev 1.00

Date: Friday, September 24, 2010 Sheet 23 of 83



## SU1F

11 FDI\_TXN0  
11 FDI\_TXP0  
11 FDI\_TXN1  
11 FDI\_TXP1  
11 FDI\_TXN2  
11 FDI\_TXP2  
11 FDI\_TXN3  
11 FDI\_TXP3  
11 FDI\_TXN4  
11 FDI\_TXP4  
11 FDI\_TXN5  
11 FDI\_TXP5  
11 FDI\_TXN6  
11 FDI\_TXP6  
11 FDI\_TXN7  
11 FDI\_TXP7

C42 FDI\_RXN0  
B43 FDI\_RXP0  
F45 FDI\_RXN1  
F43 FDI\_RXP1  
H41 FDI\_RXN2  
J41 FDI\_RXP2  
C46 FDI\_RXN3  
D47 FDI\_RXP3  
B45 FDI\_RXN4  
A46 FDI\_RXP4  
B47 FDI\_RXN5  
C49 FDI\_RXP5  
J43 FDI\_RXN6  
H43 FDI\_RXP6  
M43 FDI\_RXN7  
P43 FDI\_RXP7

## FDI

FDI\_FSYNC0  
FDI\_LSYNC0  
FDI\_FSYNC1  
FDI\_LSYNC1  
FDI\_INT

B51 FDI\_FSYNC\_0 11  
E49 FDI\_LSYNC\_0 11  
C52 FDI\_FSYNC\_1 11  
D51 FDI\_LSYNC\_1 11  
H46 FDI\_INT 11

## RSD

Reserved\_001  
DF\_TVS  
Reserved\_002  
Reserved\_003  
Reserved\_004  
Reserved\_005  
Reserved\_006  
Reserved\_007  
Reserved\_008  
Reserved\_009  
Reserved\_010  
Reserved\_011  
Reserved\_012  
Reserved\_013  
Reserved\_014  
Reserved\_015  
Reserved\_016  
Reserved\_017  
Reserved\_018  
Reserved\_019  
Reserved\_020  
Reserved\_021  
Reserved\_022  
Reserved\_023  
Reserved\_024  
Reserved\_025  
Reserved\_026  
Reserved\_027  
Reserved\_028  
Reserved\_029

AB50 TP\_NVR\_DATA0  
Y40 TP\_NVR\_DATA1  
AB49 TP\_NVR\_DATA2  
AB44 TP\_NVR\_DATA3  
U49 TP\_NVR\_DATA4  
R44 TP\_NVR\_DATA5  
U50 TP\_NVR\_DATA6  
U44 TP\_NVR\_DATA7  
H50 TP\_NVR\_DATA8  
K46 TP\_NVR\_DATA9  
L56 TP\_NVR\_DATA10  
J55 TP\_NVR\_DATA11  
E53 TP\_NVR\_DATA12  
H52 TP\_NVR\_DATA13  
E52 TP\_NVR\_DATA14  
R50 TP\_NVR\_DATA15  
TP\_SU1\_029

ST105 NOBOM  
ST106 NOBOM  
ST107 NOBOM  
ST108 NOBOM  
ST109 NOBOM  
ST110 NOBOM  
ST111 NOBOM  
ST112 NOBOM  
ST113 NOBOM  
ST114 NOBOM  
ST115 NOBOM  
ST116 NOBOM  
ST117 NOBOM  
ST118 NOBOM  
ST119 NOBOM  
ST120 NOBOM  
ST129 NOBOM

## CLOCK

CLKOUT\_ITPXPDP\_N  
CLKOUT\_ITPXPDP\_P  
CLKOUT\_DMI1\_N  
CLKOUT\_DMI1\_P  
CLKOUT\_DP\_N  
CLKOUT\_DP\_P

R52 CK\_100M\_CPUXDP# 82  
N52 CK\_100M\_CPUXDP 82  
P31 CK\_100M\_DMI# 12  
R31 CK\_100M\_DMI 12  
N56 TP\_CLKOUT\_DP# CLKOUT\_BCLK# 1  
M55 TP\_CLKOUT\_DP# CLKOUT\_BCLK# 1

ST40 NOBOM  
ST41 NOBOM

CLKOUT\_PCIE7N  
CLKOUT\_PCIE7P  
CLKOUT\_PCIE6N  
CLKOUT\_PCIE6P  
CLKOUT\_PCIE5N  
CLKOUT\_PCIE5P

AE2 CK\_100M\_USB3# 39  
AE1 CK\_100M\_USB3 39  
AB3 CK\_100M\_PCHXDP# 83  
AA2 CK\_100M\_PCHXDP 83  
AF3 CK\_100M\_BRIDGE# 47  
AG2 CK\_100M\_BRIDGE 47

Y9 CK\_100M\_PE2# 34  
Y8 CK\_100M\_PE2 34  
AB9 CK\_100M\_PE3# 34  
AB8 CK\_100M\_PE3 34  
AB12 CK\_100M\_LAN# 35  
AB14 CK\_100M\_LAN 35  
AA5 CK\_100M\_SATA3# 51  
W5 CK\_100M\_SATA3 51

CLKOUT\_PCIE4N  
CLKOUT\_PCIE4P  
CLKOUT\_PCIE3N  
CLKOUT\_PCIE3P  
CLKOUT\_PCIE2N  
CLKOUT\_PCIE2P

AE6 TP\_CPU\_AE6  
AC6 TP\_CPU\_AC6

ST42 NOBOM  
ST43 NOBOM

CLKOUT\_PEG\_A\_N  
CLKOUT\_PEG\_A\_P  
CLKOUT\_PEG\_B\_N  
CLKOUT\_PEG\_B\_P

AE12 TP\_CLKOUT\_PEG\_B#  
AE11 TP\_CLKOUT\_PEG\_B

ST54 NOBOM  
ST55 NOBOM

CLKOUT\_PCIO  
CLKOUT\_PC1  
CLKOUT\_PC2  
CLKOUT\_PC3  
CLKOUT\_PC4

AT11 IPD\_20K PCH\_CLKOUT\_PCIO  
AN14 IPD\_20K PCH\_CLKOUT\_PC1  
AT12 IPD\_20K PCH\_CLKOUT\_PC2  
AT17 IPD\_20K PCH\_CLKOUT\_PC3  
AT14 IPD\_20K PCH\_CLKOUT\_PC4

SR251 1 2 22 OHM  
SR277 1 2 22 OHM  
ST164 NOBOM  
ST253 1 2 22 OHM

CLKOUT\_FLEX0/GPIO64  
CLKOUT\_FLEX1/GPIO65  
CLKOUT\_FLEX2/GPIO66  
CLKOUT\_FLEX3/GPIO67

AT9 IPD\_20K CLKOUT\_FLEX0 GPIO64  
BA5 IPD\_20K PCH\_CLKOUT\_FLEX1 48M SIO  
AW5 IPD\_20K CLKOUT\_FLEX0 GPIO66  
BA2 IPD\_20K CLKOUT\_FLEX0 GPIO67

ST57 NOBOM  
SR152 1 2 22 OHM  
ST163 NOBOM  
ST163 NOBOM

CK\_33M\_SIO 53  
CK\_33M\_DEBUG 80  
CK\_33M\_TPM 55  
CK\_33M\_PCIFB 19

CK\_48M\_SIO 53

## NOTE:

1. Prioritize 27/14/24/48/25-MHz FLEX on FLEX1/3.
2. Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0/2 if more than 2 PCI clocks + PCI loopback are routed.
3. With 2 PCI clocks routed (or less), prioritize the FLEX clocks to FLEX1/3
  - a. 27MHz(SSC/non-SSC)
  - b. 14.31818MHz
  - c. 24/48
  - d. 25MHz

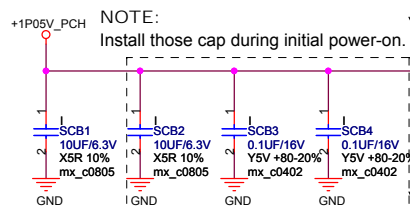
PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title : CLK/NVRAM/FDI 6-9

Pegatron Corp. Engineer: *Livy\_Zhu*

Size A3	Project Name <b>IPMSB-BE/CR</b>	Rev 1.00
Date: Friday, September 24, 2010	Sheet 24 of 83	

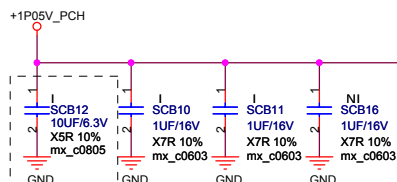




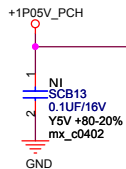
NOTE:  
Splitting 2 power trace/shape  
on pin Y20/Y22/V22 to other pins.

NOTE:  
Trace needs  
to be at least  
20 mils width  
with full VSS/  
VCC reference  
plane

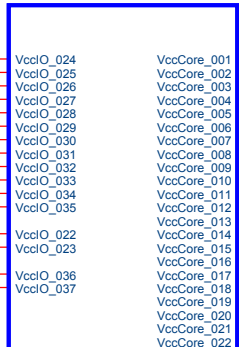
NOTE:  
Splitting 2 power trace/shape



NOTE:  
Install SCB12 during initial power-on.



SU1G



VccIO\_024

VccIO\_025

VccIO\_026

VccIO\_027

VccIO\_028

VccIO\_029

VccIO\_030

VccIO\_031

VccIO\_032

VccIO\_033

VccIO\_034

VccIO\_035

VccIO\_036

VccIO\_037

VccIO\_022

VccIO\_023

VccIO\_008

VccIO\_009

VccIO\_010

VccIO\_019

VccIO\_020

VccIO\_021

VccIO\_007

VccIO\_011

VccASW\_004

VccASW\_005

VccASW\_006

VccASW\_007

VccASW\_008

VccASW\_009

VccASW\_010

VccASW\_011

VccASW\_012

VccASW\_013

VccASW\_014

VccASW\_015

VccASW\_016

VccASW\_017

VccASW\_018

VccASW\_019

VccASW\_020

VccASW\_021

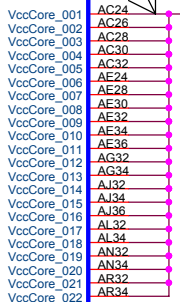
VccASW\_022

VccASW\_023

VccASW\_003

VccASW\_002

VccASW\_001



VccCore\_001

VccCore\_002

VccCore\_003

VccCore\_004

VccCore\_005

VccCore\_006

VccCore\_007

VccCore\_008

VccCore\_009

VccCore\_010

VccCore\_011

VccCore\_012

VccCore\_013

VccCore\_014

VccCore\_015

VccCore\_016

VccCore\_017

VccCore\_018

VccCore\_019

VccCore\_020

VccCore\_021

VccCore\_022

VccCore\_023

VccCore\_024

VccCore\_025

VccCore\_026

VccCore\_027

VccCore\_028

VccCore\_029

VccCore\_030

VccCore\_031

VccCore\_032

VccCore\_033

VccCore\_034

VccCore\_035

VccCore\_036

VccCore\_037

VccCore\_038

VccCore\_039

VccCore\_040

VccCore\_041

VccCore\_042

VccCore\_043

VccCore\_044

VccCore\_045

VccCore\_046

VccCore\_047

NOTE:  
Splitting 2 power trace/shape  
on pins AV24/AV26 to AY25/AY27,  
and AE40 to AG38/AG40.

NOTE:  
Splitting 2 power traces  
on pins AC20 to AE20.

NOTE:  
VccAFDIPLL and VccACik  
can be NC in on-die VR mode.

VccAFDIPLL

VccACik

VccAPLLEXP

VccAPLLSATA

VccAPLLDMI2

VccCLKDMI

VccADAC

VccADPLL

VccADPLLB

VccADPLLB

VccADPLLB

VccADPLLB

VccADPLLB

VccADPLLB

VccADPLLB

VccADPLLB

VccADPLLB

VccADPLLB

VccADPLLB

VccADPLLB

VccADPLLB

VccADPLLB

+1P05V\_PCH

+1P05V\_PCH

+1P05V\_PCH

+1P05V\_PCH

+1P05V\_PCH

+1P05V\_PCH

+1P05V\_PCH

+1P05V\_PCH

+1P05V\_PCH

+1P05V\_PCH

+1P05V\_PCH

+1P05V\_PCH

+1P05V\_PCH

+1P05V\_PCH

+1P05V\_PCH

+1P05V\_PCH

+1P05V\_PCH

+1P05V\_PCH

+1P05V\_PCH

+1P05V\_PCH

+1P05V\_PCH

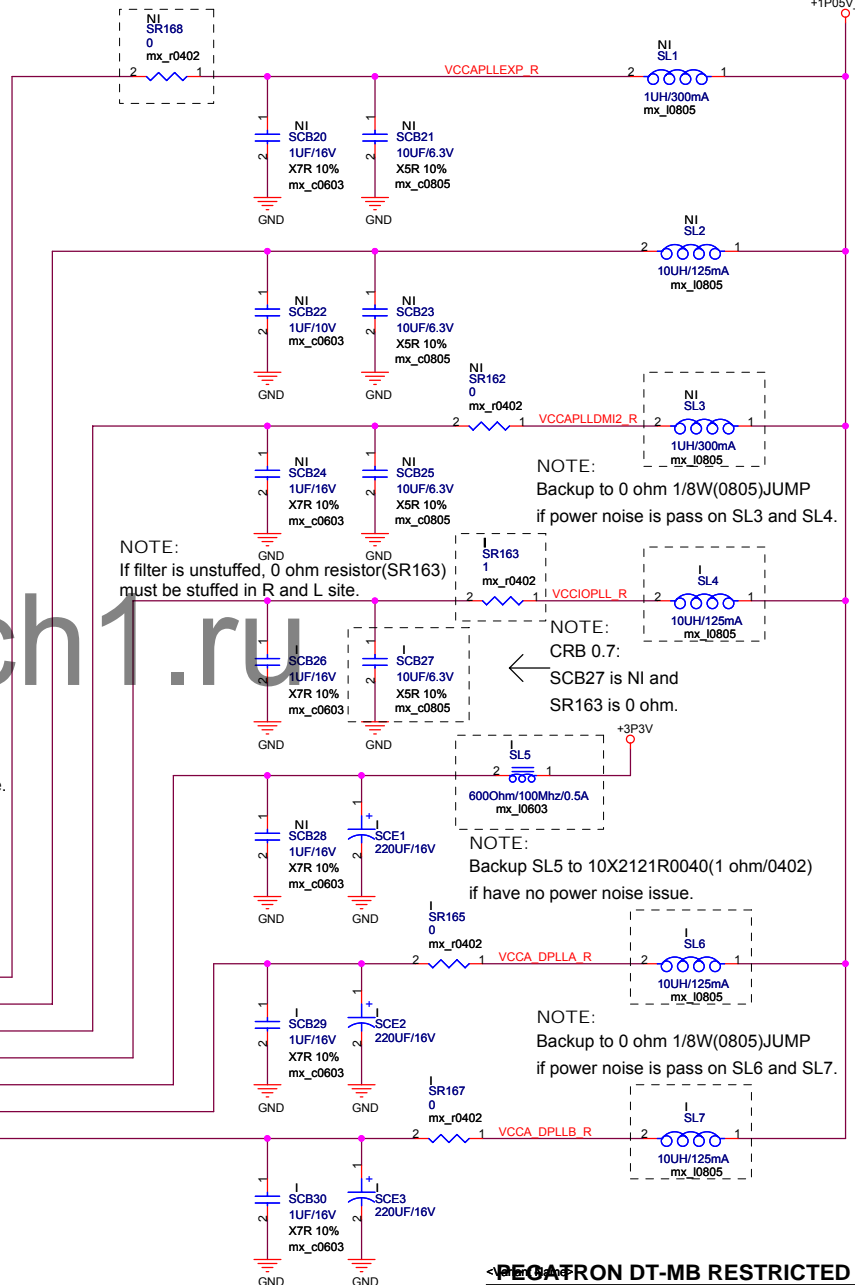
+1P05V\_PCH

+1P05V\_PCH

+1P05V\_PCH

+1P05V\_PCH

NOTE:  
VccAPLLEXP, VccAPLLSATA, and VccAPLLDMI2 can be NC  
in On-Die VR mode.



NOTE:  
Backup to 0 ohm 1/8W(0805)JUMP  
if power noise is pass on SL3 and SL4.

NOTE:  
If filter is unstuffed, 0 ohm resistor(SR163)  
must be stuffed in R and L site.

NOTE:  
CRB 0.7:  
SCB27 is NI and  
SR163 is 0 ohm.

NOTE:  
Backup SL5 to 10X2121R0040(1 ohm/0402)  
if have no power noise issue.

NOTE:  
Backup to 0 ohm 1/8W(0805)JUMP  
if power noise is pass on SL6 and SL7.

PEGATRON DT-MB RESTRICTED SECRET

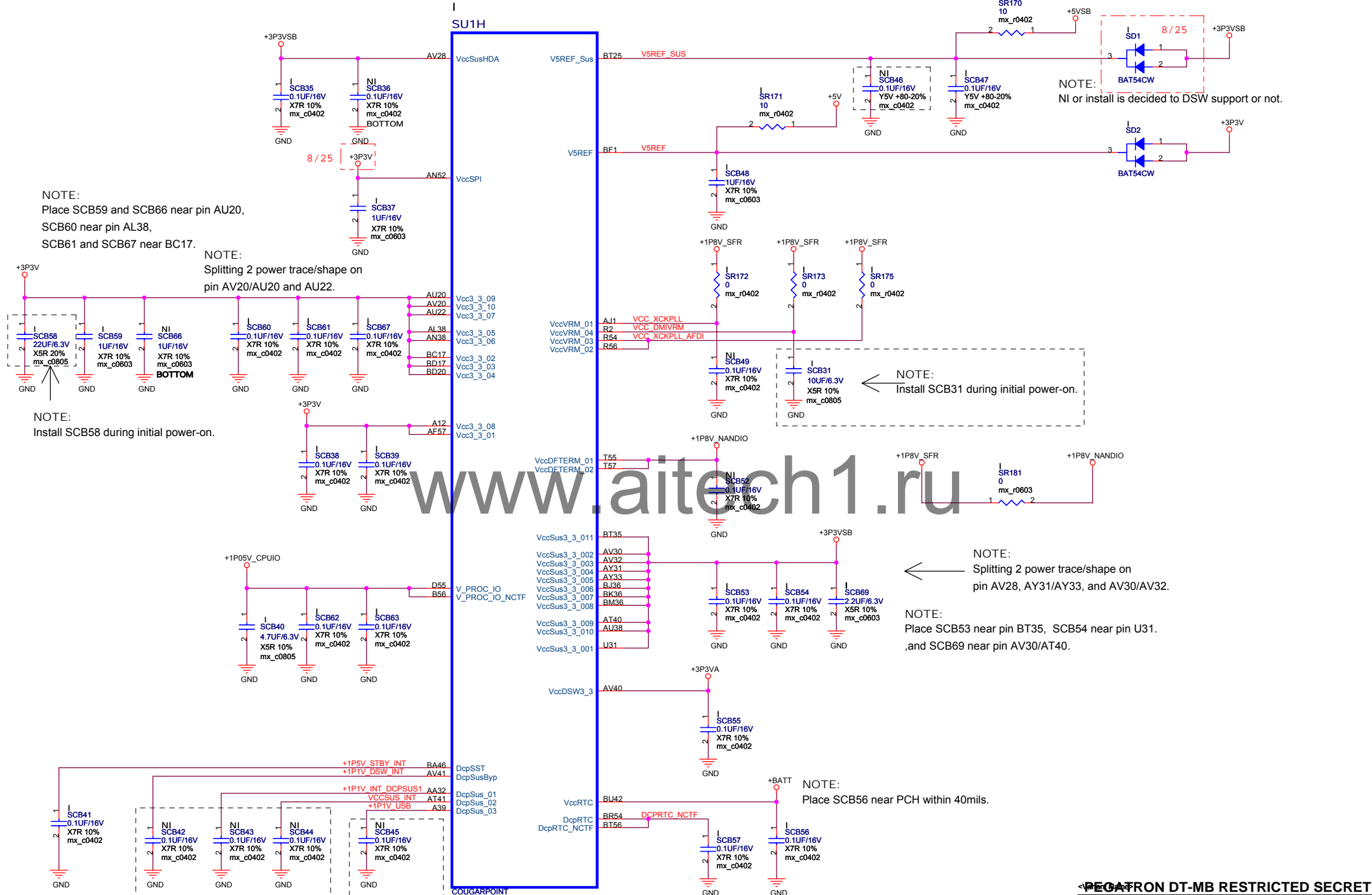
PEGATRON Title : VCC/PLL 7-9

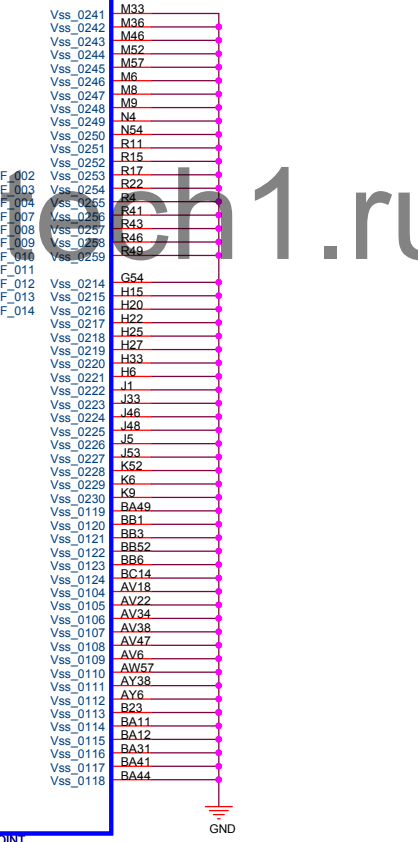
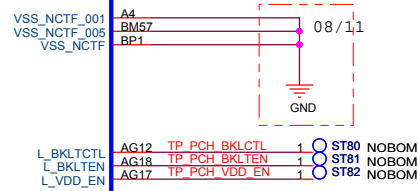
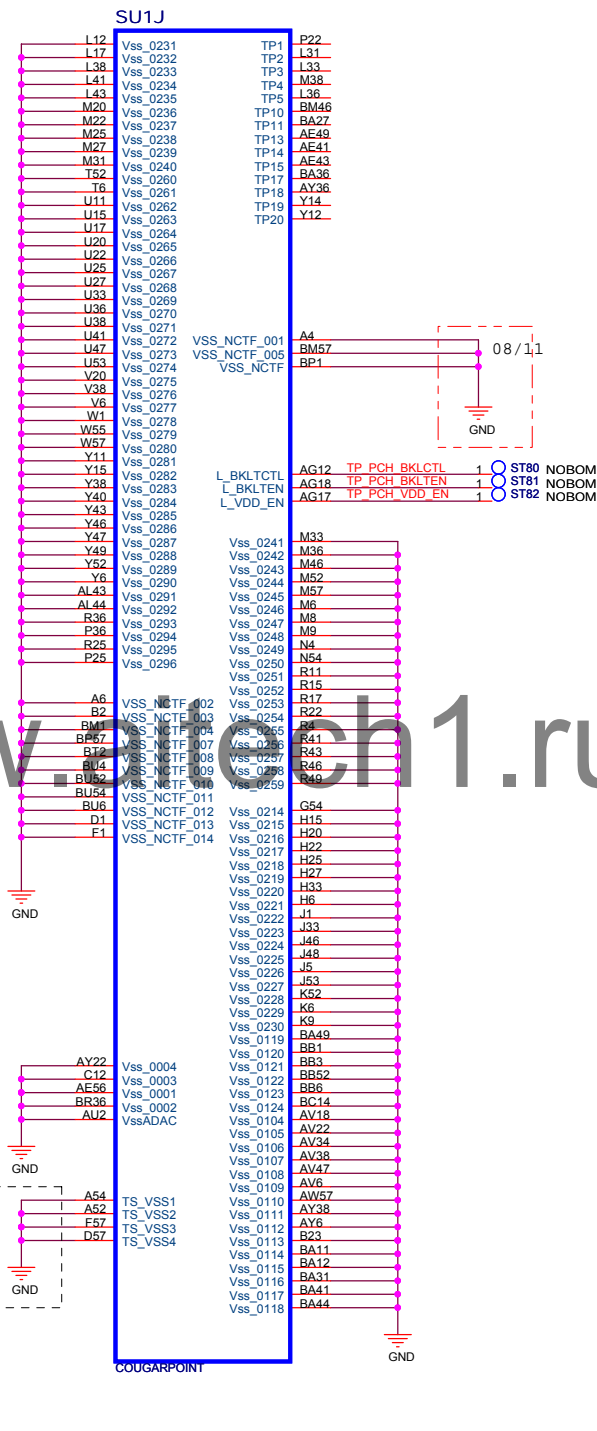
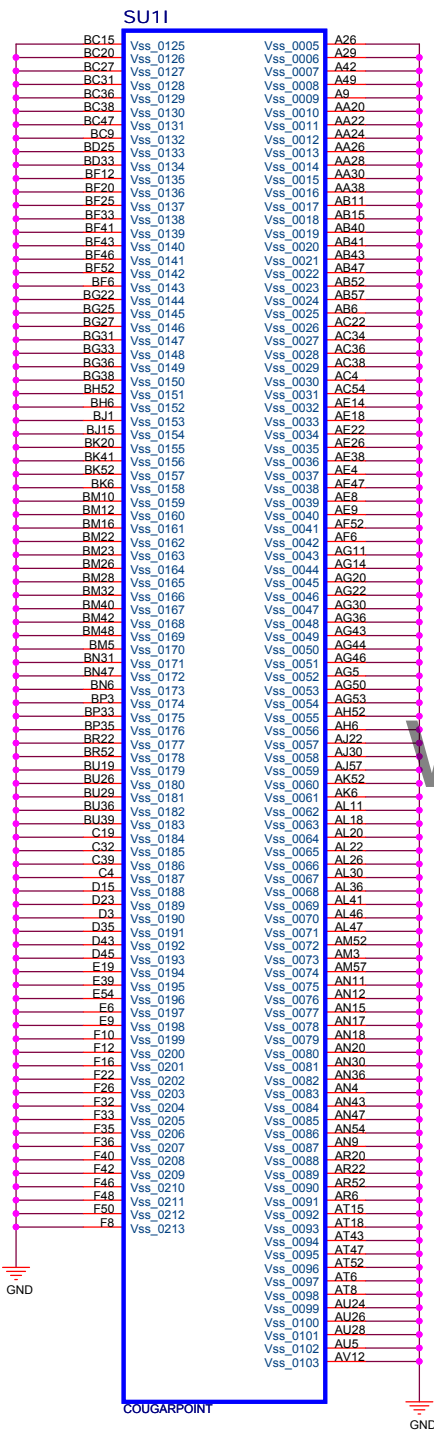
Pegatron Corp. Engineer: Liny\_Zhu

Size A3 Project Name IPMSB-BE/CR

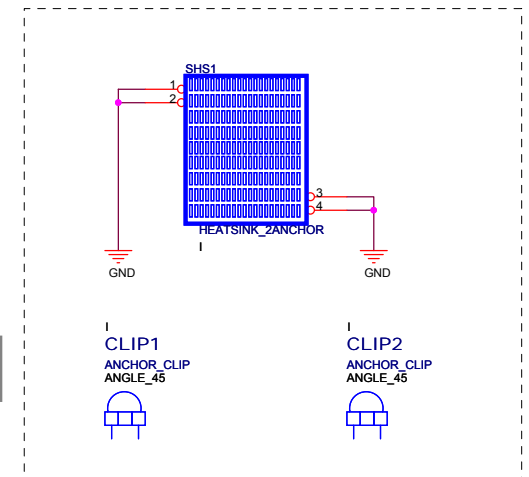
Date: Friday, September 24, 2010 Sheet 25 of 83

Rev 1.00

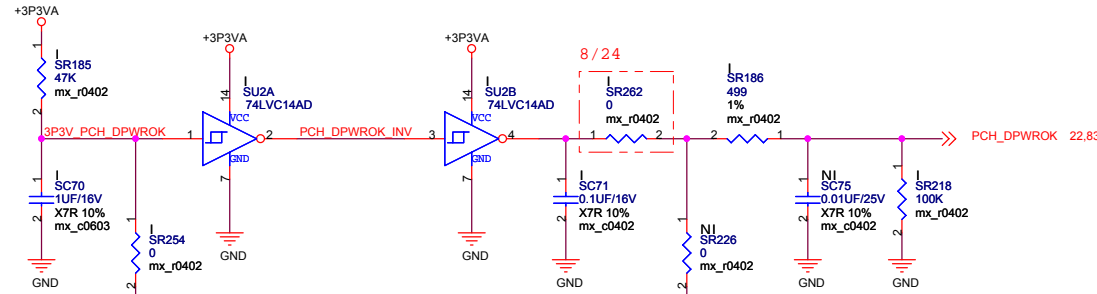




NOTE:  
BOM option depend on thermal result

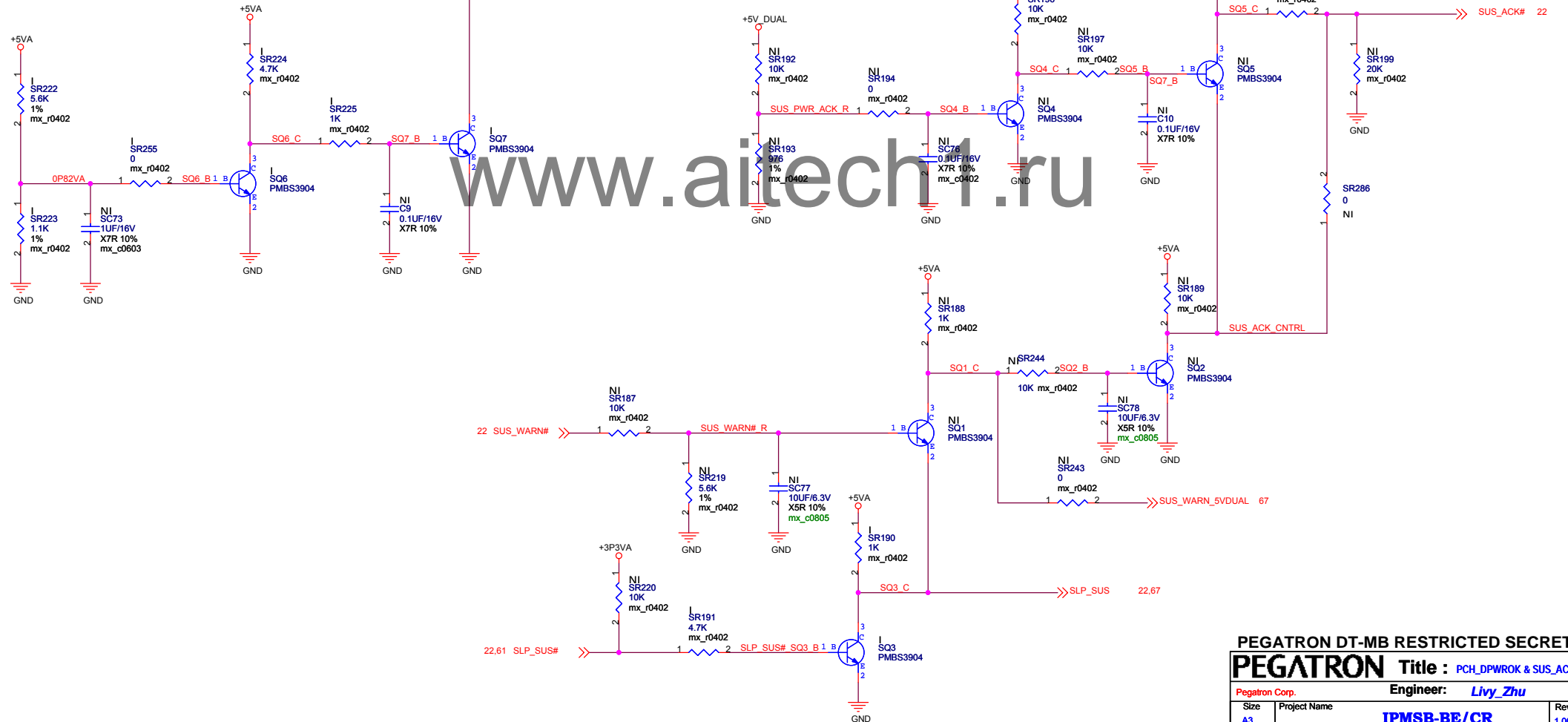


# PCH\_DPWROK



# SUS\_ACK#

NOTE:  
Check voltage level of SUS\_ACK# of PCH  
and decide resistor value of SR199.



PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title : PCH\_DPWROK & SUS\_ACK#

Pegatron Corp. Engineer: *Livy\_Zhu*

Size A3	Project Name <b>IPMSB-BE/CR</b>	Rev 1.00
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Date: Friday, September 24, 2010 Sheet 28 of 83

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PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title :

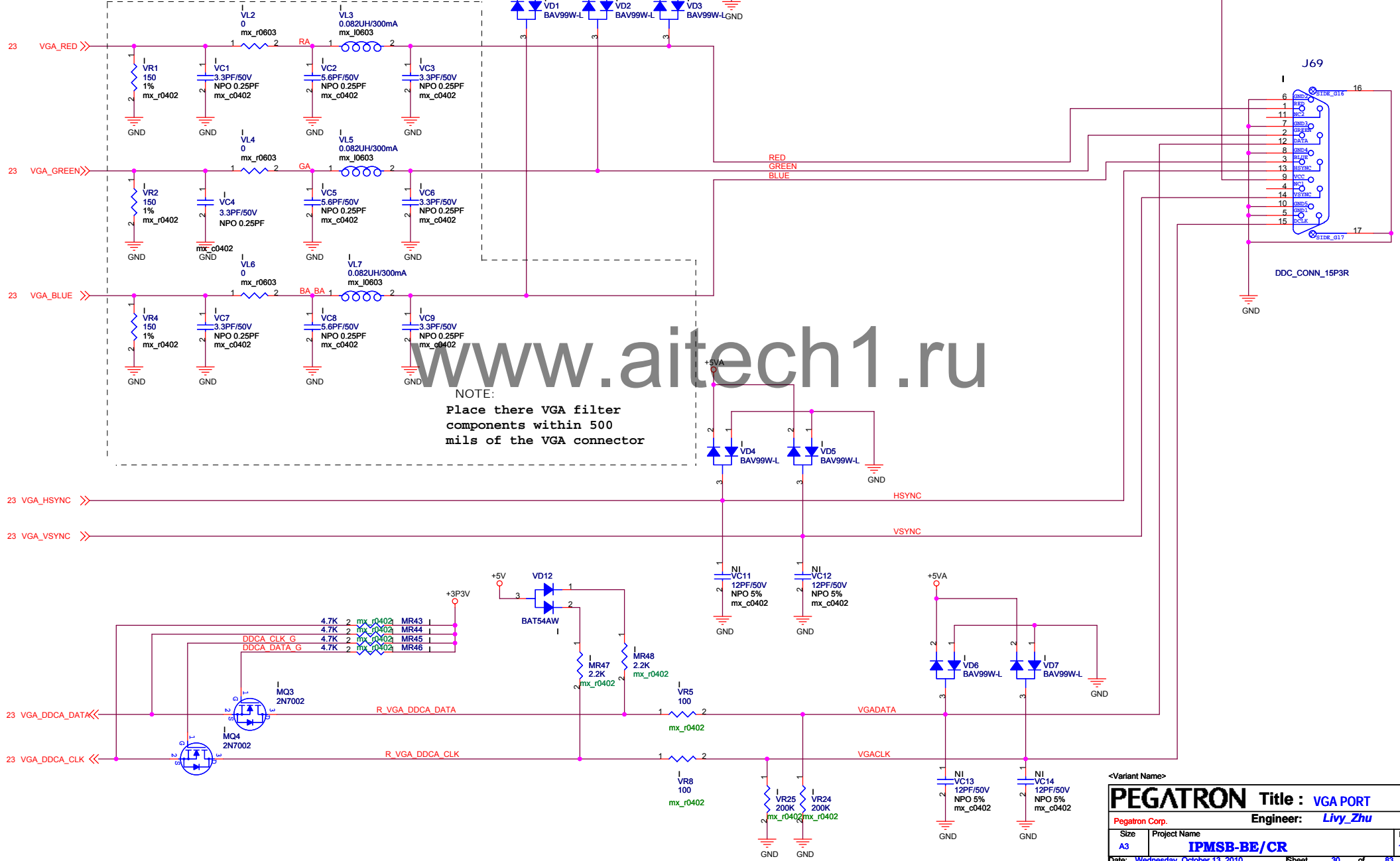
Pegatron Corp. Engineer: *Livy\_Zhu*

Size A3	Project Name <b>IPMSB-BE/CR</b>	Rev 1.00
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Date: *Friday, September 24, 2010* Sheet 29 of 83

Install the VD1/VD2/VD3/VD4/VD5 diode to prevent from ESD issue

NOTE:



NOTE:  
Place there VGA filter  
components within 500  
mils of the VGA connector

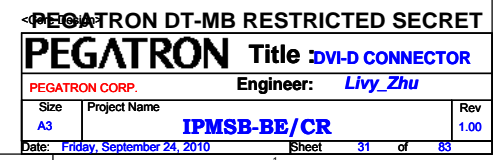
<Variant Name>

**PEGATRON** Title : **VGA PORT**

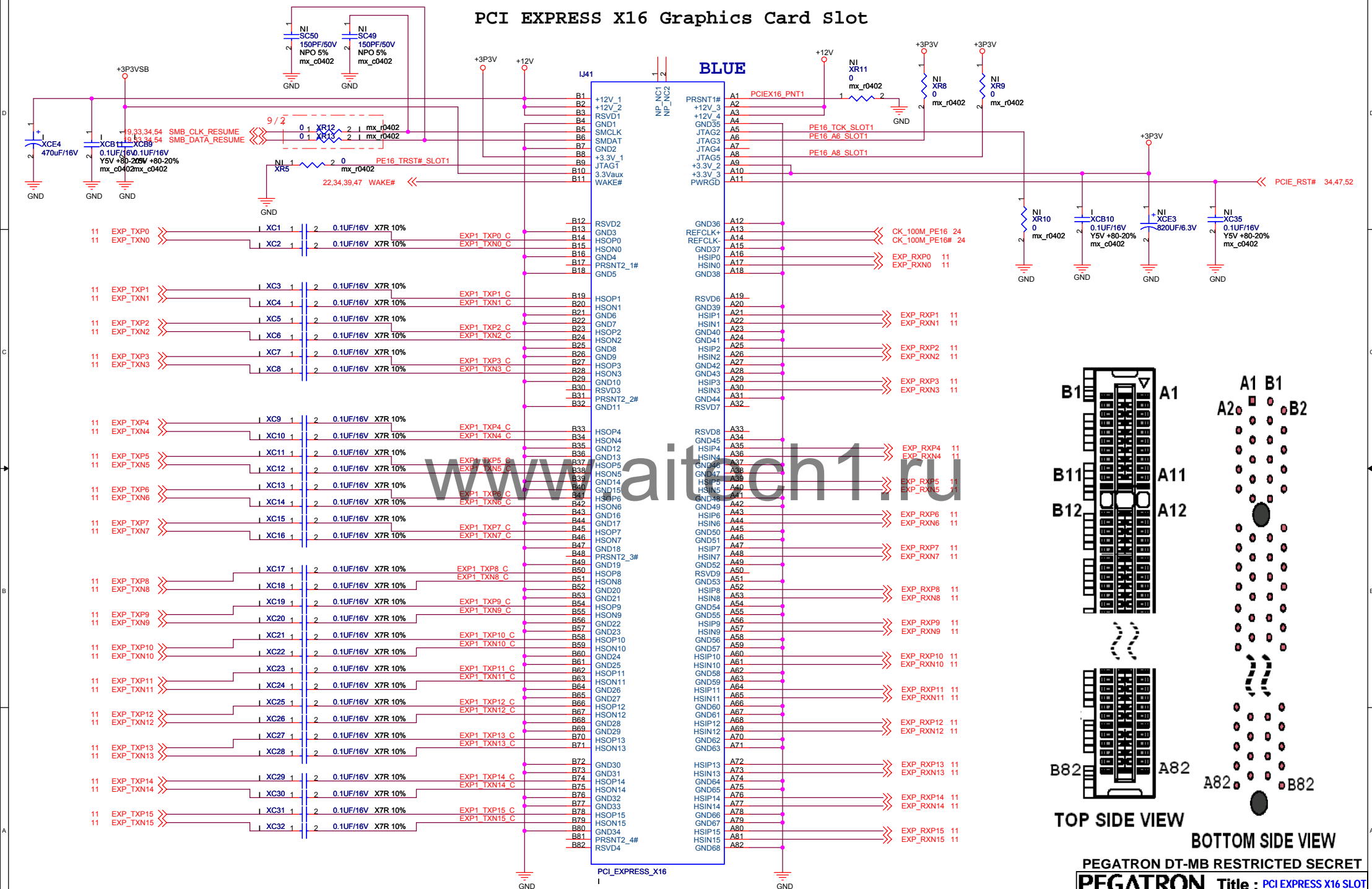
Pegatron Corp. Engineer: **Livy\_Zhu**

Size A3	Project Name <b>IPMSB-BE/CR</b>	Rev 1.00
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Date: Wednesday, October 13, 2010 Sheet 30 of 83



PCI EXPRESS X16 Graphics Card Slot



**TOP SIDE VIEW**

**BOTTOM SIDE VIEW**

**PEGATRON DT-MB RESTRICTED SECRET**

**PEGATRON** Title : PCI EXPRESS X16 SLOT

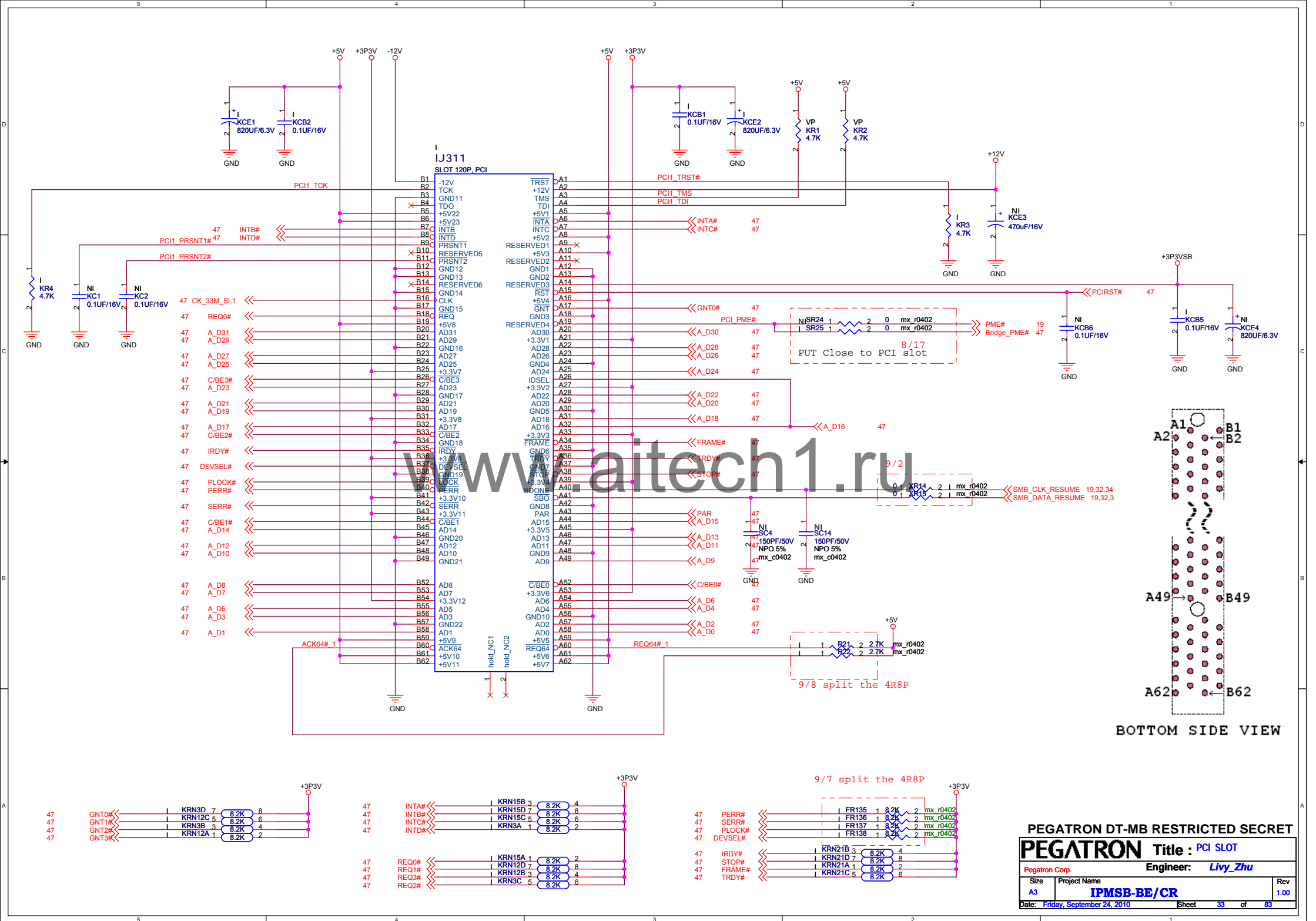
Pegatron Corp. Engineer: *Livy\_Zhu*

Size A3	Project Name IPMSB-BE/CB	Rev 1.00
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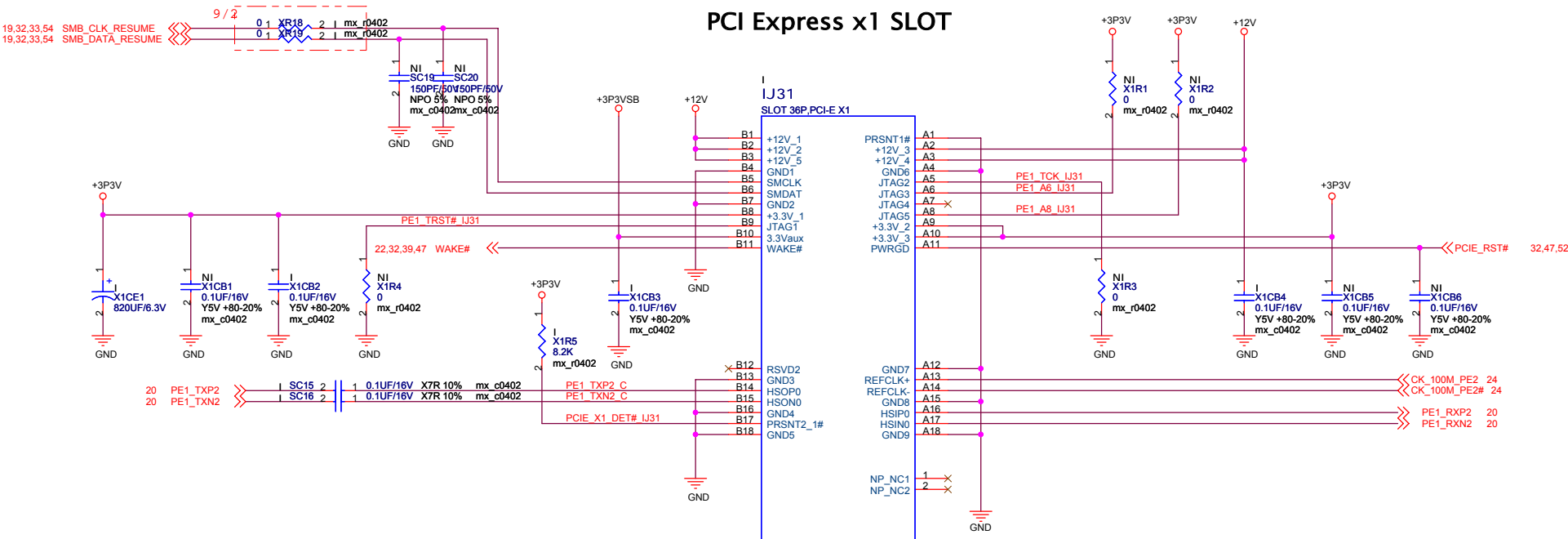
Date: Friday, September 24, 2010 Sheet 32 of 83

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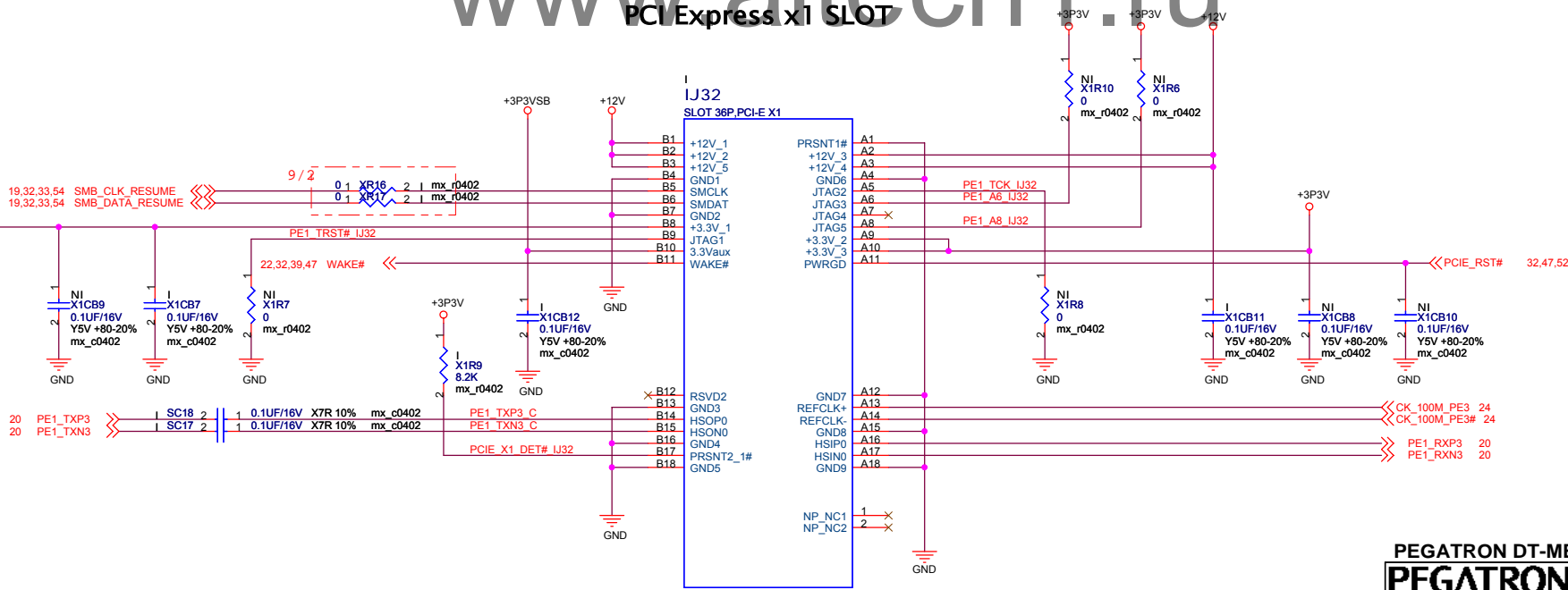


# PCI Express x1 SLOT

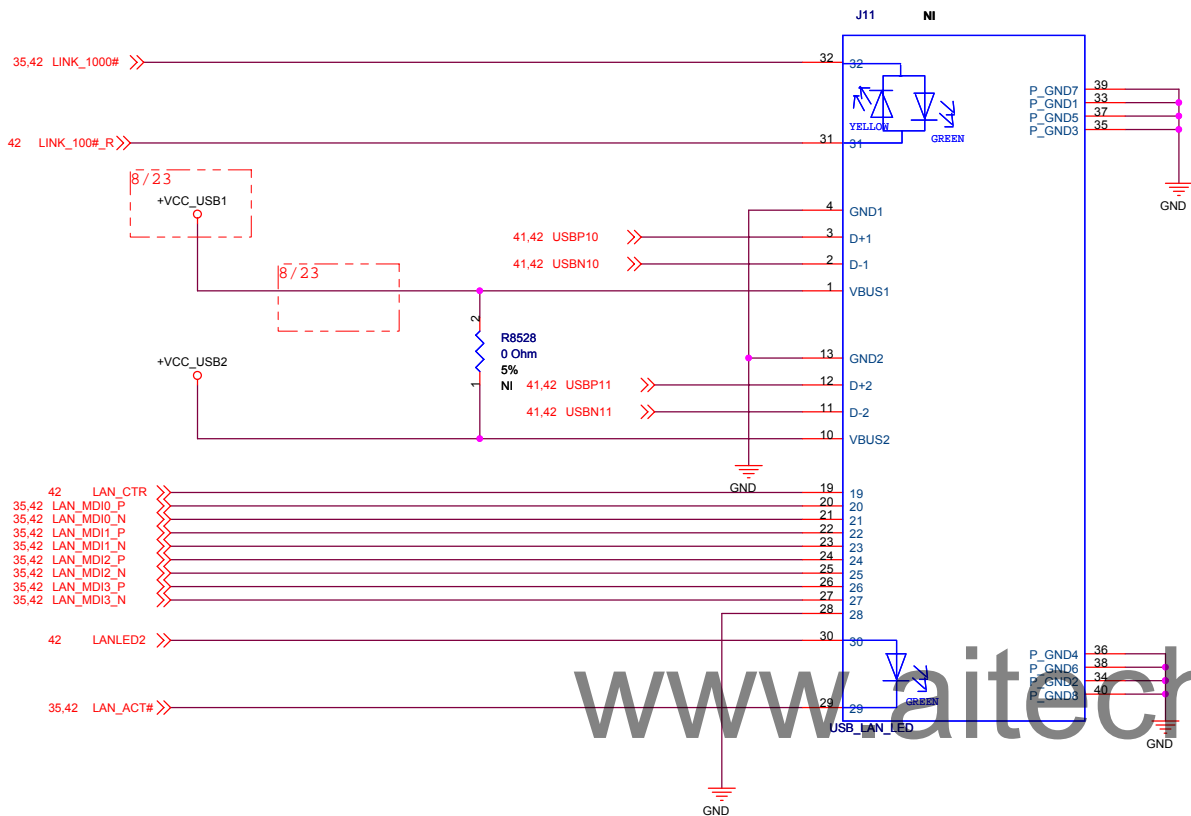


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# PCI Express x1 SLOT







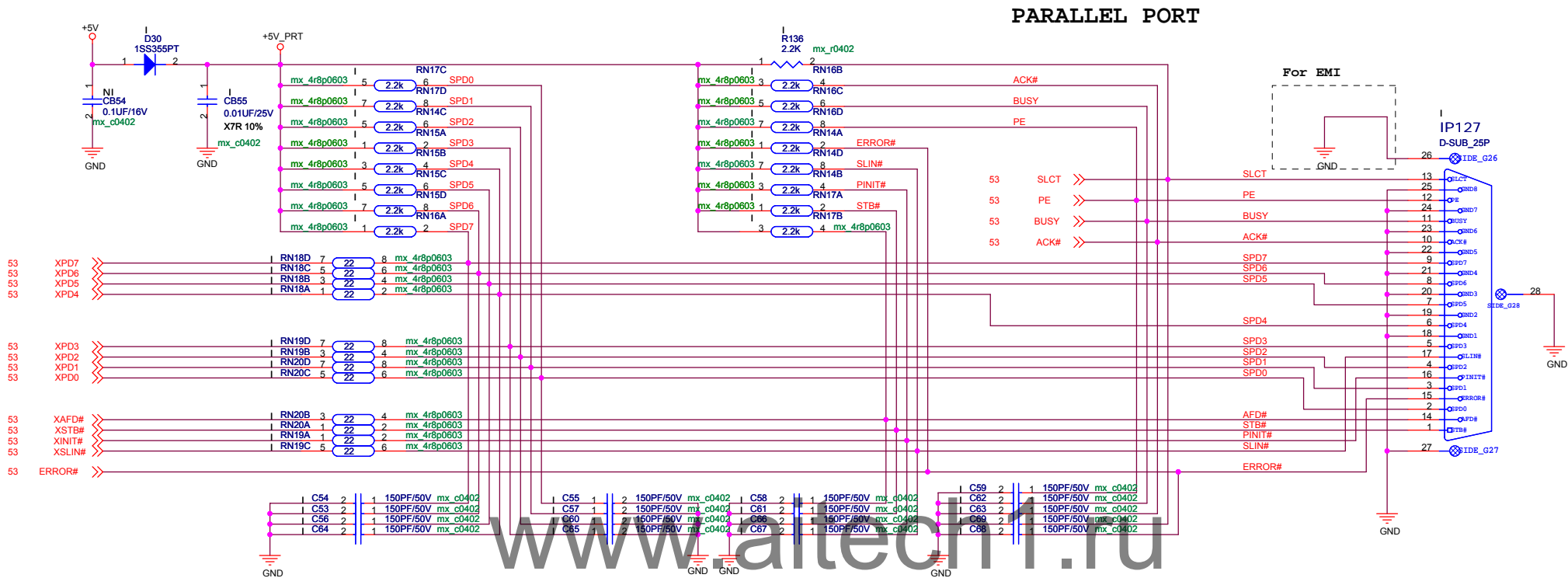
www.aitech1.ru

PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title : RJ45+USB2.0

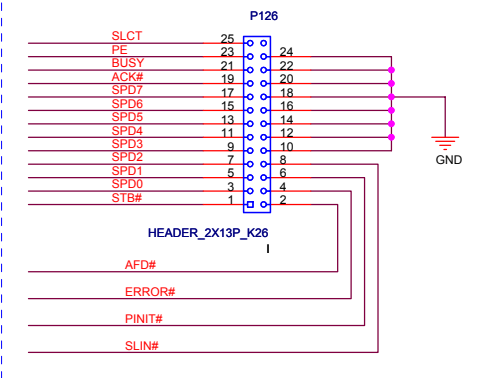
PEGATRON CORP. Engineer: Livy\_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00
Date: Friday, September 24, 2010	Sheet 36 of 83	



08/13: NI LPT header From Fab.B

8/18:  
change LPT header from 12X60202DB10 to 12X60202DIW0



PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title : PRINT PORT

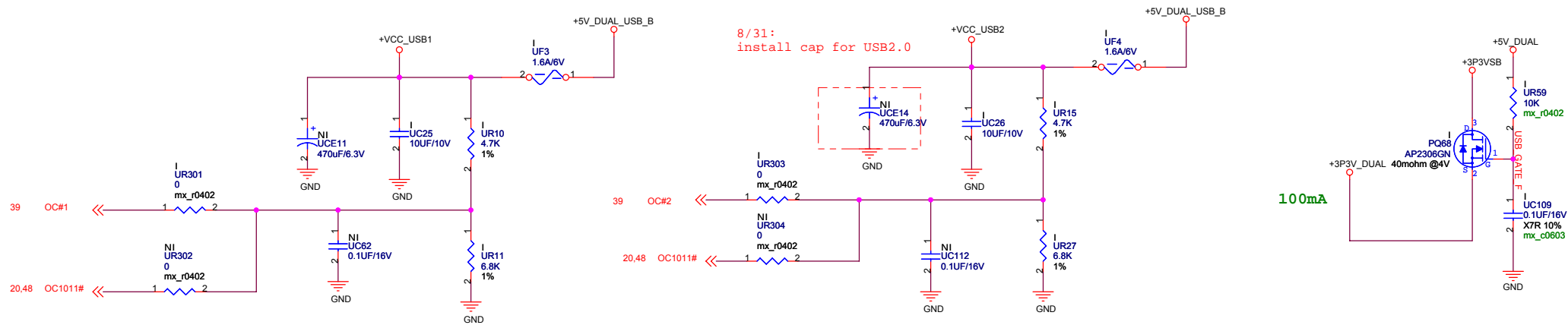
Pegatron Corp. Engineer: Livy\_Zhu

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 37 of 83



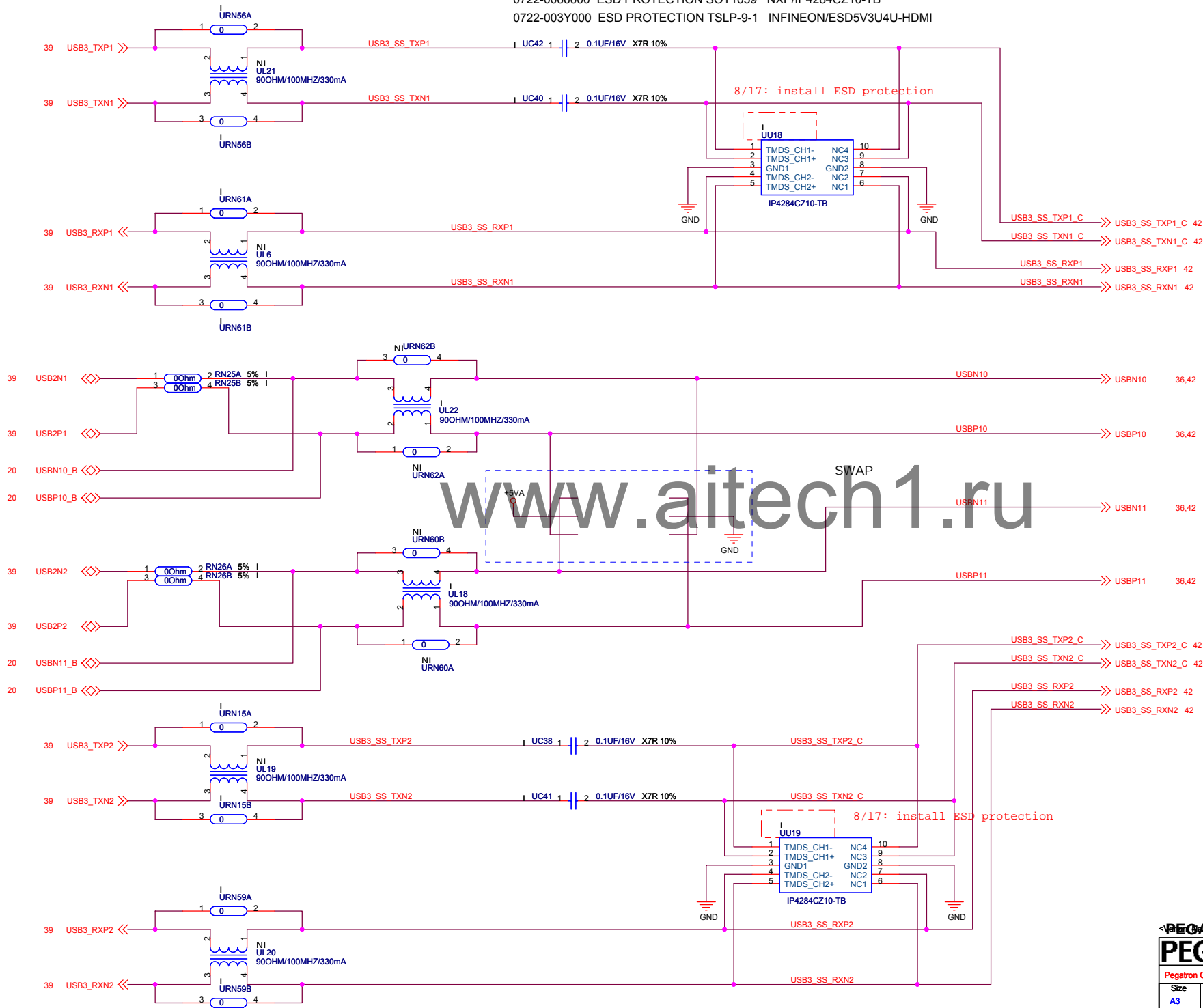


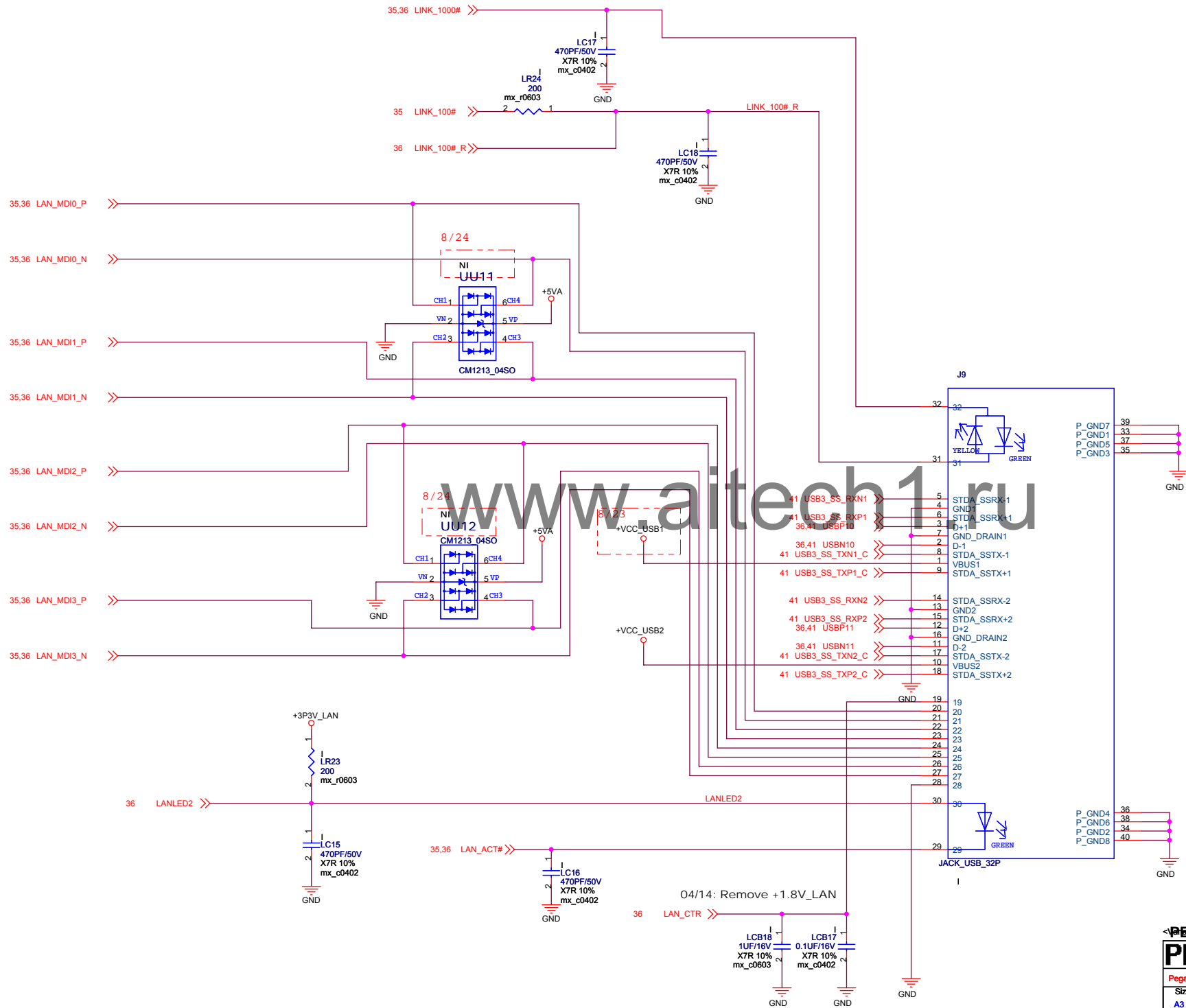


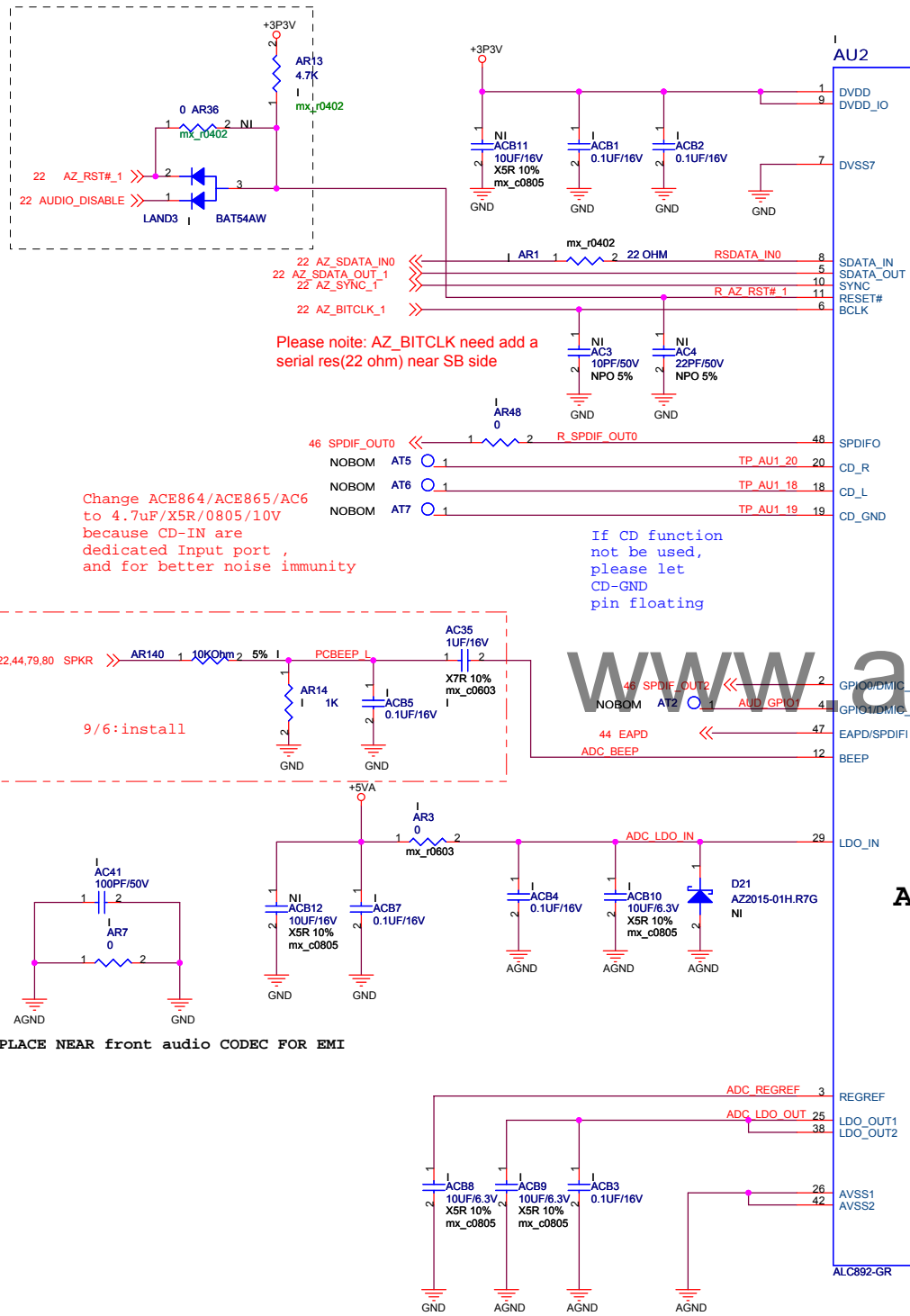
www.aitech1.ru



NOTE:  
0722-0066000 ESD PROTECTION SOT1059 NXP/IP4284CZ10-TB  
0722-003Y000 ESD PROTECTION TSLP-9-1 INFINEON/ESD5V3U4U-HDMI







If pin 23/24 and pin 21/22 support retasking function, please changed AR34/AR35/AR30/AR31 to 75 ohm

If front Microphone is not support retasking function, 1.ACE8/ACE9 can be changed to SMD 4.7uF(11X234475150) 2.please change AR4/AR6 to 1K for better ESD immunity

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ALC892

# INTERNAL SPEAKER HEADER

43 MONO\_OUT >>  
SPKR:  
From Audio CODEC

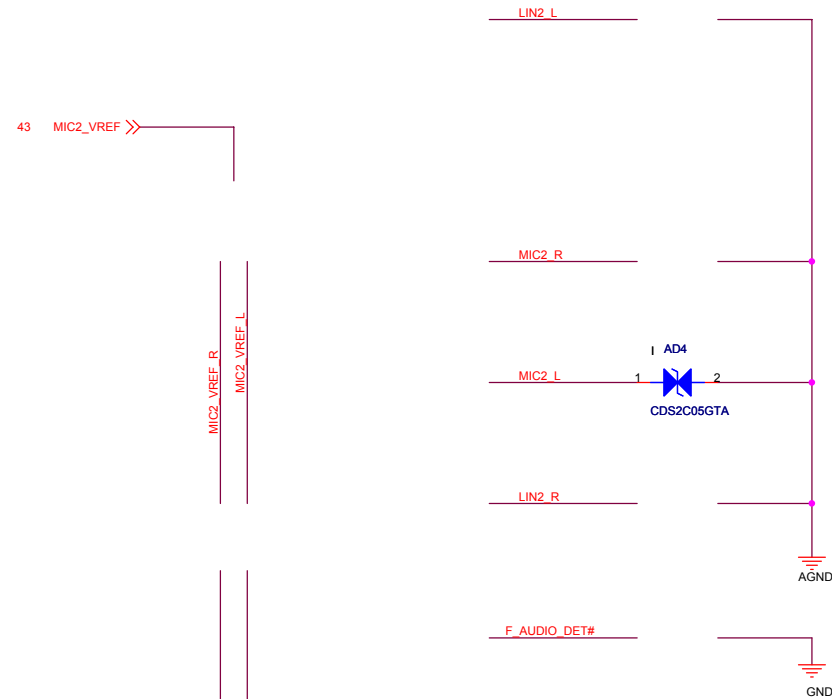
Note:(Layout)  
Please add some GND vias on thermal pad

22,43,79,80 SPKR >>  
SPKR:  
From PCH

MUTE#:  
Please select a GPO pin from SB or SIO  
43 EAPD >> NI 1 2 AR49  
mx\_r0402

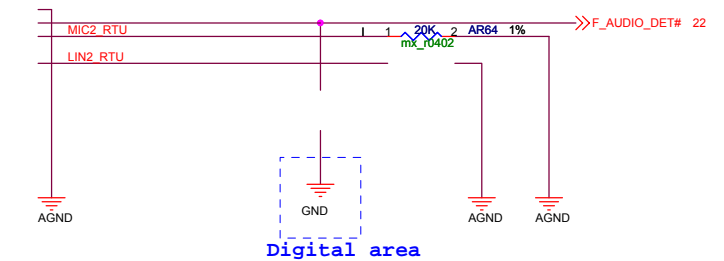
Net	Level	H Level	L Level
Mute#	Non-Mute	Mute	
AZ_GPI00#	Non-Mute	Mute	

The SSM22113 is a high performance audio amplifier that delivers 1 W rms of low distortion audio power into a bridgeconnected 8 Ω speaker load (or 1.5 W rms into 4 Ω load).

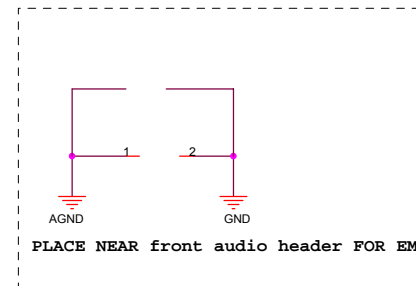


## Front Audio Header

YELLOW



If front HP-OUT is not support retasking,  
these Vreference circuit can be removed.

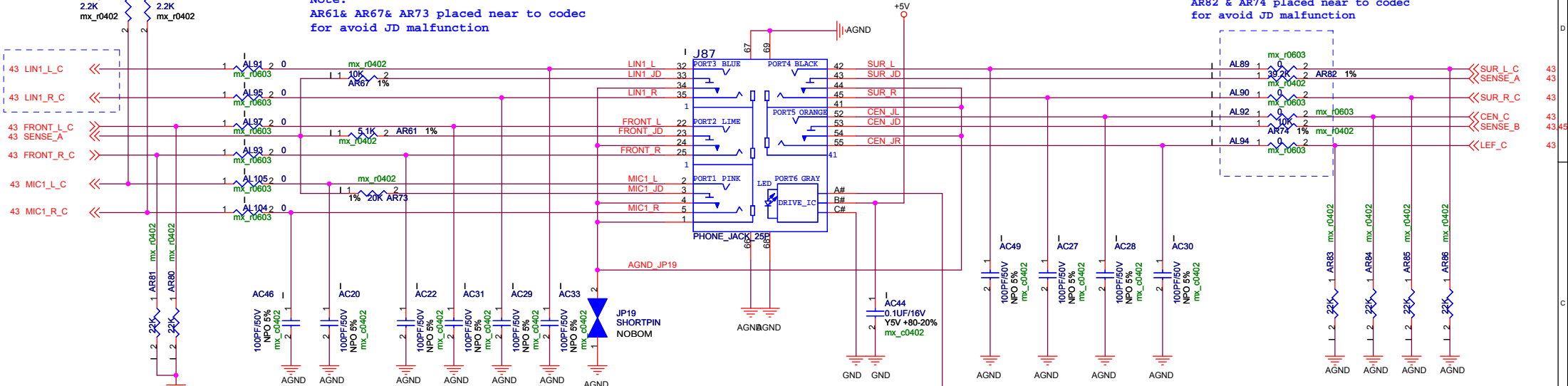


AL87/AL89/AL91/AL93/AL95/AL97; Please use  
09X131216000 instead of 0 ohm if you found have  
EMI issue

## Azalia Rear Audio Connector

Note:  
AR61& AR67& AR73 placed near to codec  
for avoid JD malfunction

Note:  
AR82 & AR74 placed near to codec  
for avoid JD malfunction

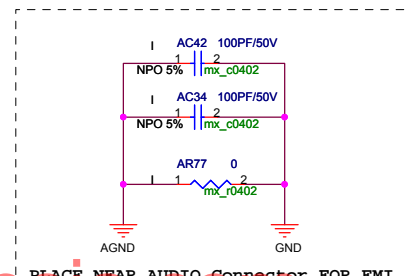
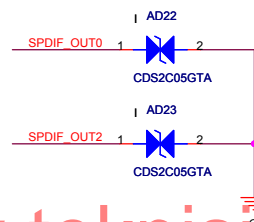
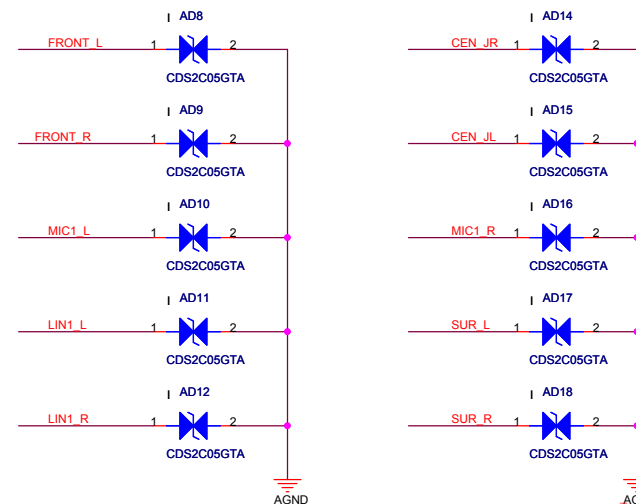
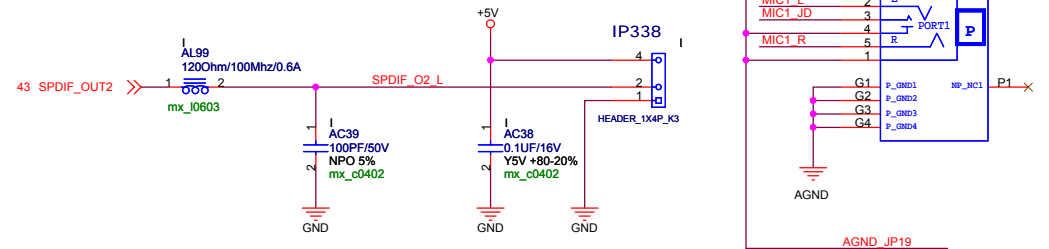


Note(CD\_IN\_JD):  
If LINE1(PIN23/24) are used  
to be rear Line-in port ,  
please change this connection to  
"SENSE\_A"(serial resistor : 10K)

If for HP CPC 6+3 configuration  
just keep "CD\_IN\_JD"

AL88/AL90/AL92/AL94/AL96/AL98; Please use  
09X131216000 instead of 0 ohm if you found have  
EMI issue

## SPDIF OUT2 CONNECTOR



PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title : REAL AUDIO CONN

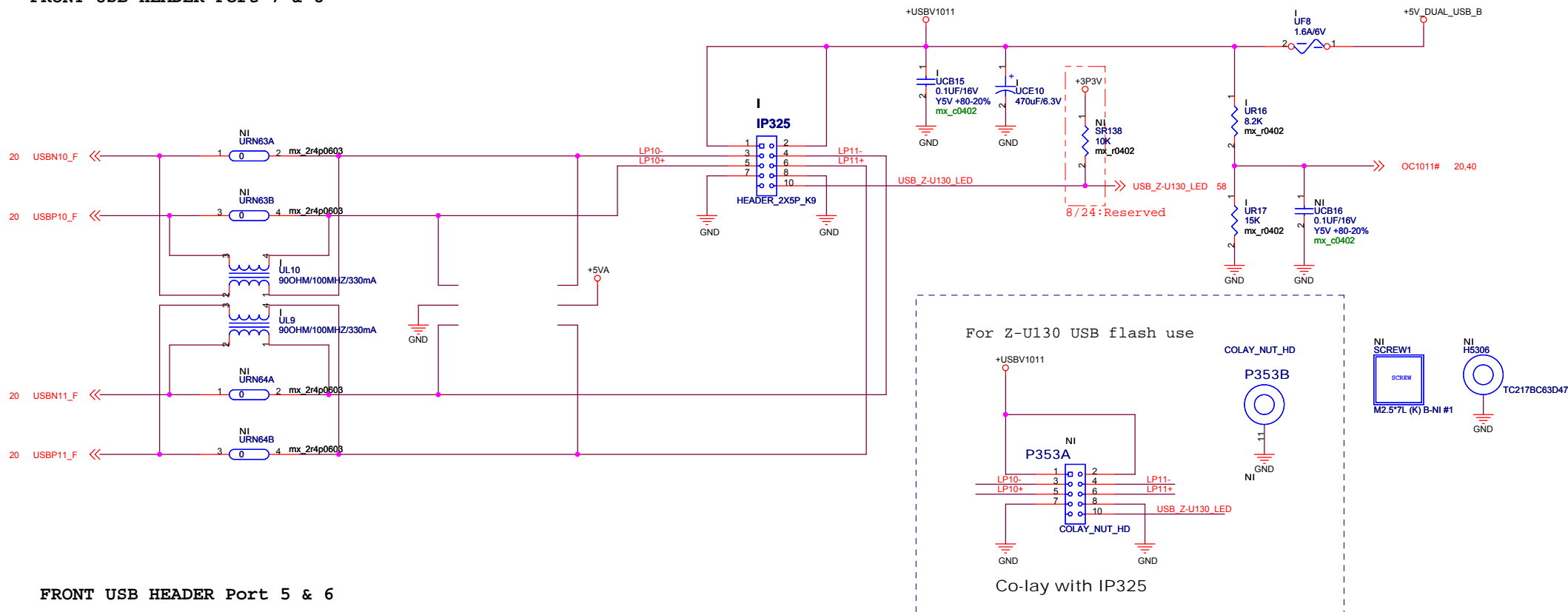
Pegatron Corp. Engineer: *Livy\_Zhu*

Size A3 Project Name **IPMSB-BE/CR** Rev 1.00

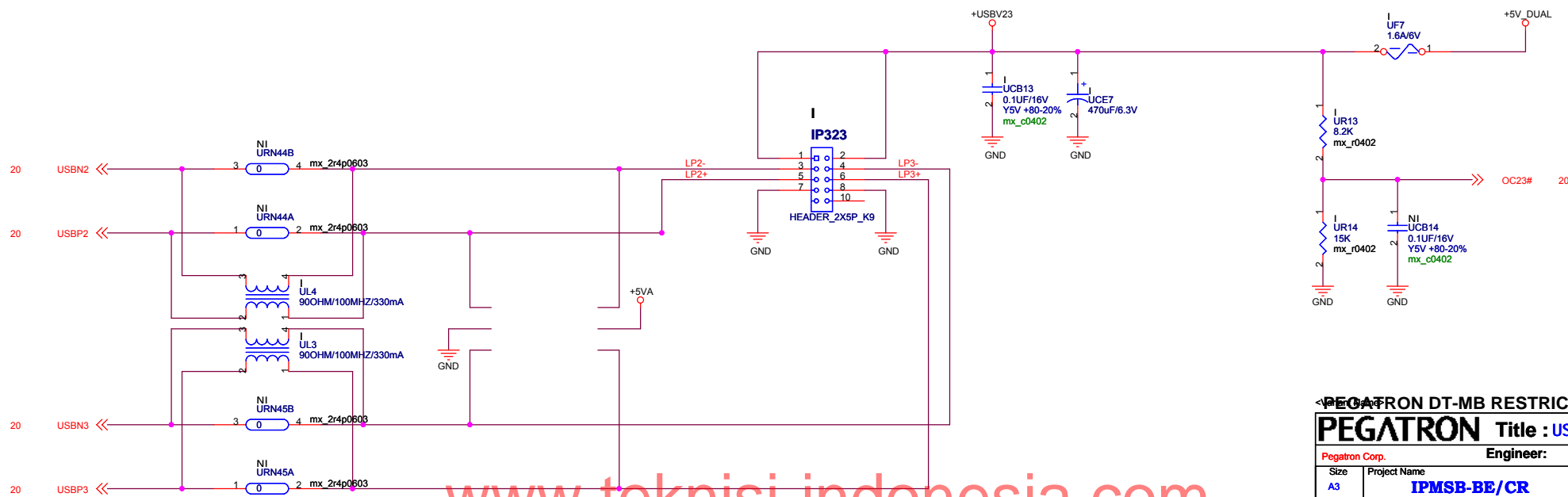
Date: Friday, September 24, 2010 Sheet 46 of 83



# FRONT USB HEADER Port 7 & 8

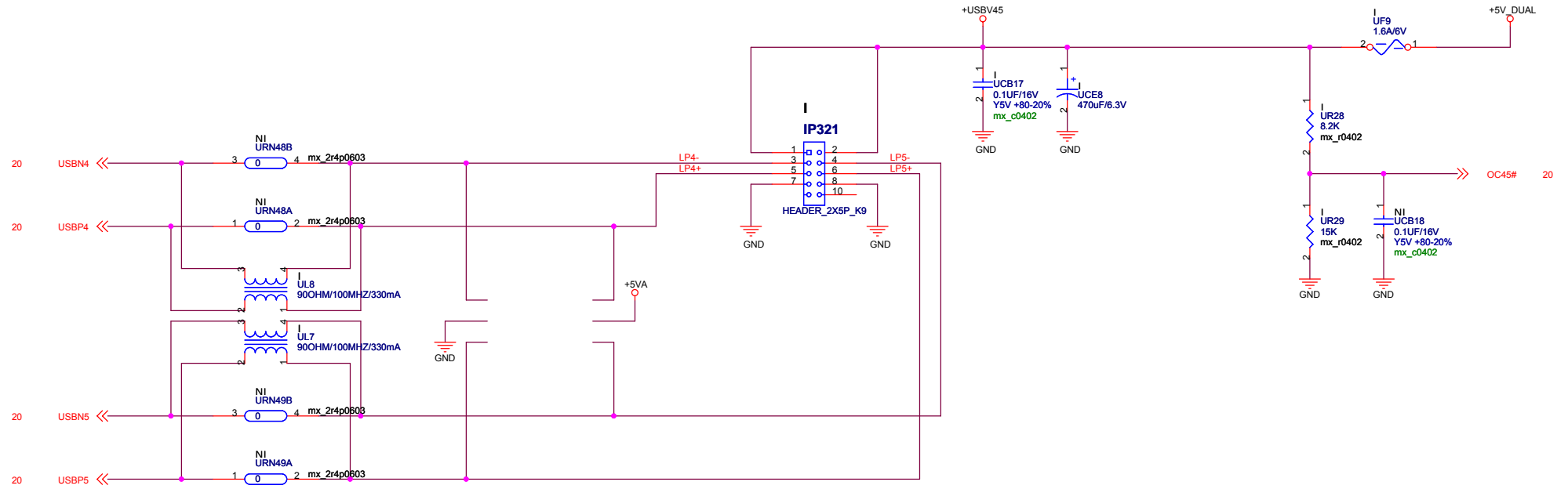


# FRONT USB HEADER Port 5 & 6

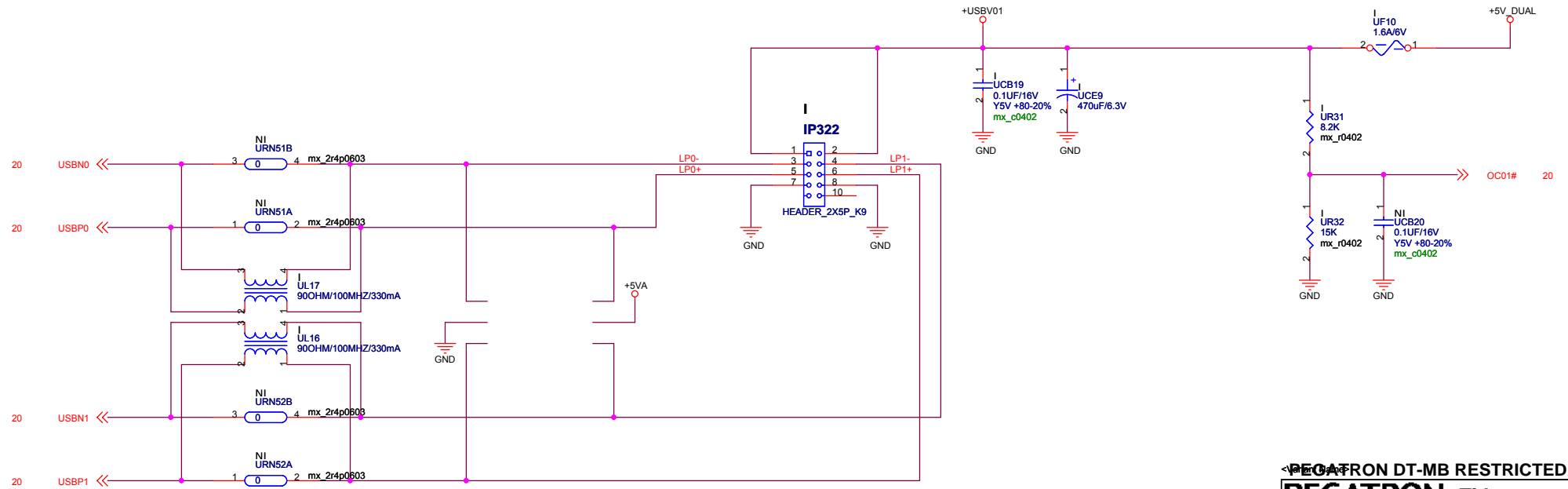




## FRONT USB HEADER Port 1 & 2



## FRONT USB HEADER Port 3 & 4

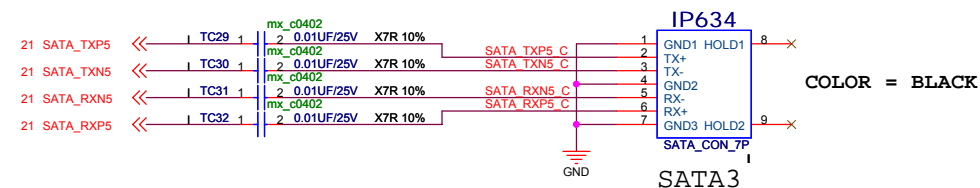
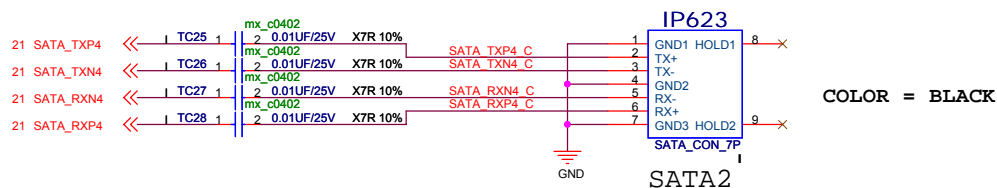
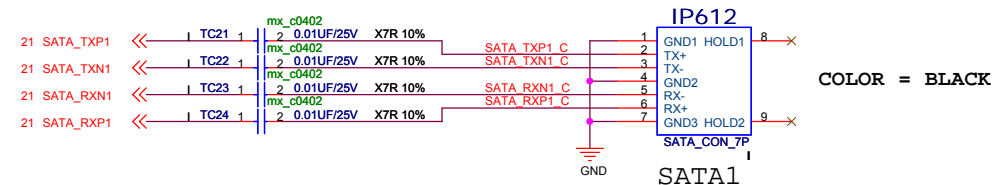
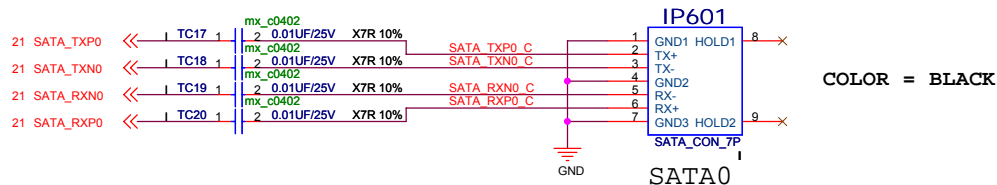


PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title : USB HEADER-2

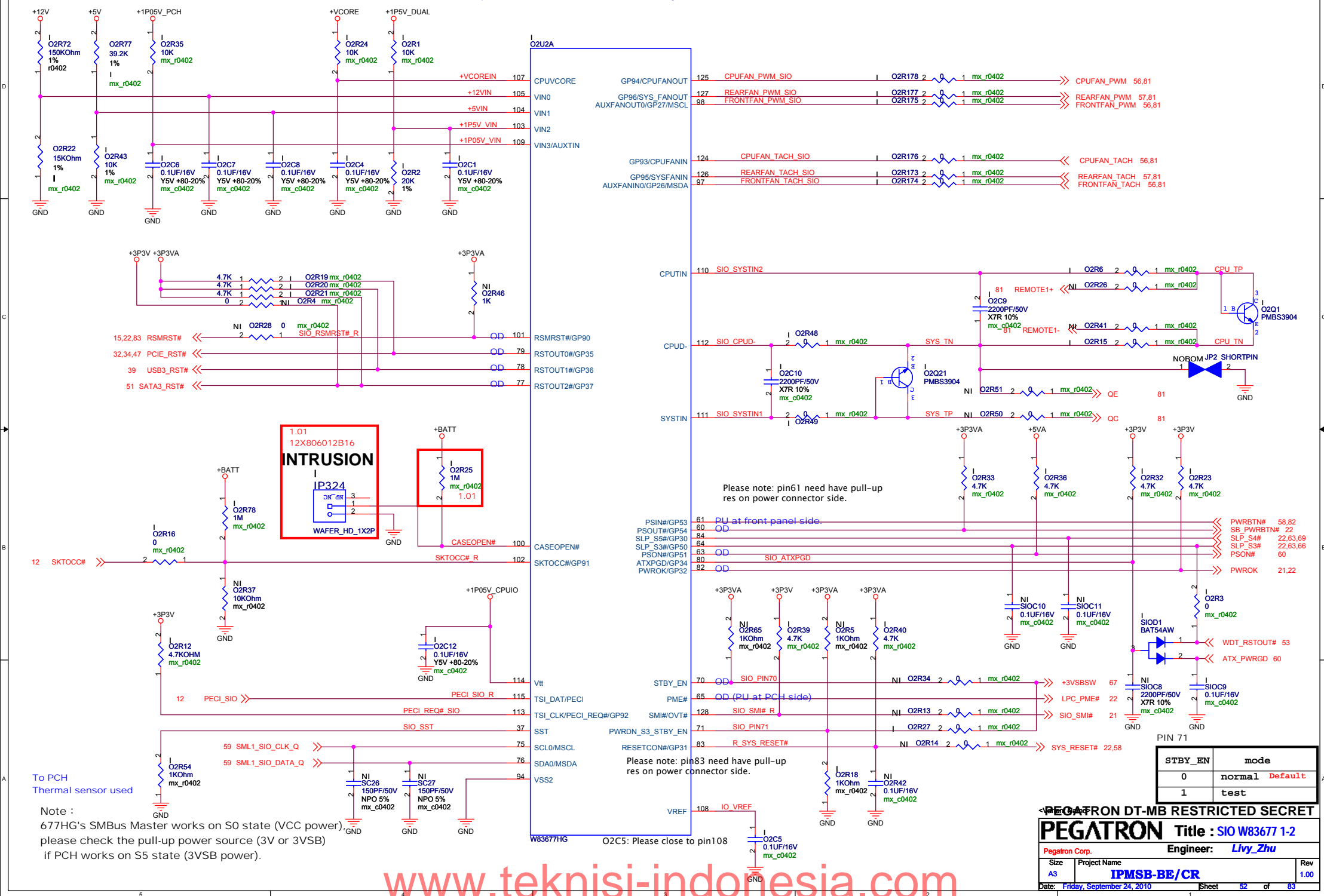
Pegatron Corp. Engineer: *Livy\_Zhu*

Size A3	Project Name IPMSB-BE/CR	Rev 1.00
Date: Friday, September 24, 2010	Sheet 49 of 83	





Please do not leave pin 103 VCORE\_REFIN floating.  
Otherwise, pin 63 PSON# will be affected and the system cannot be booted.

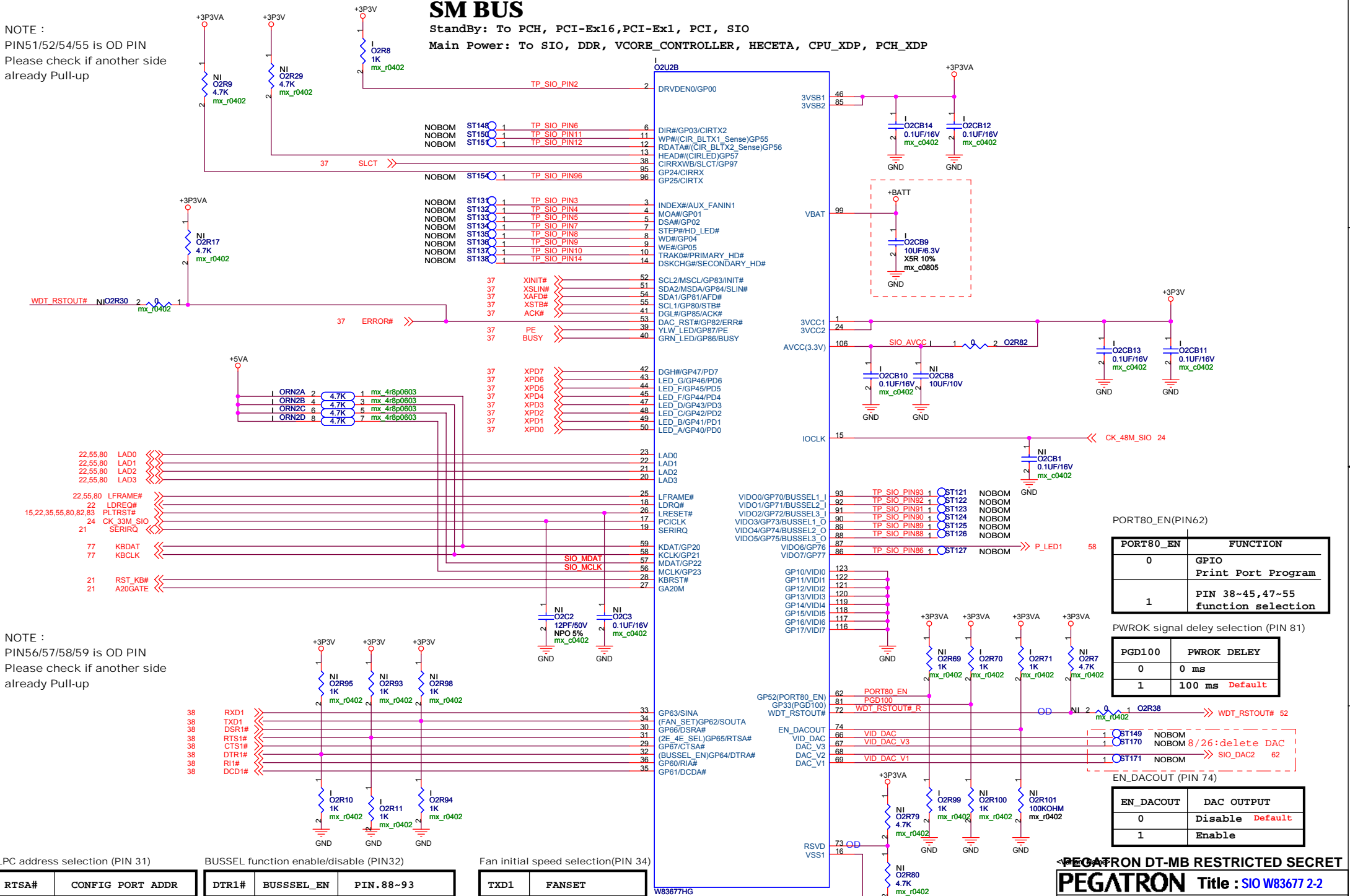


NOTE :  
PIN51/52/54/55 is OD PIN  
Please check if another side  
already Pull-up

# SM BUS

StandBy: To PCH, PCI-Ex16, PCI-Ex1, PCI, SIO

Main Power: To SIO, DDR, VCORE\_CONTROLLER, HECETA, CPU\_XDP, PCH\_XDP



NOTE :  
PIN56/57/58/59 is OD PIN  
Please check if another side  
already Pull-up

LPC address selection (PIN 31)

RTSA#	CONFIG	PORT ADDR
0	0x002E	Default
1	0x004E	

BUSSEL function enable/disable (PIN32)

DTR1#	BUSSEL_EN	PIN.88~93
0	DISABLE	VIDO
1	ENABLE	BUSSEL IN/OUT

Fan initial speed selection(PIN 34)

TXD1	FANSET
0	50% Default
1	100%

PORT80_EN	FUNCTION
0	GPIO Print Port Program
1	PIN 38~45,47~55 function selection

PWROK signal deley selection (PIN 81)

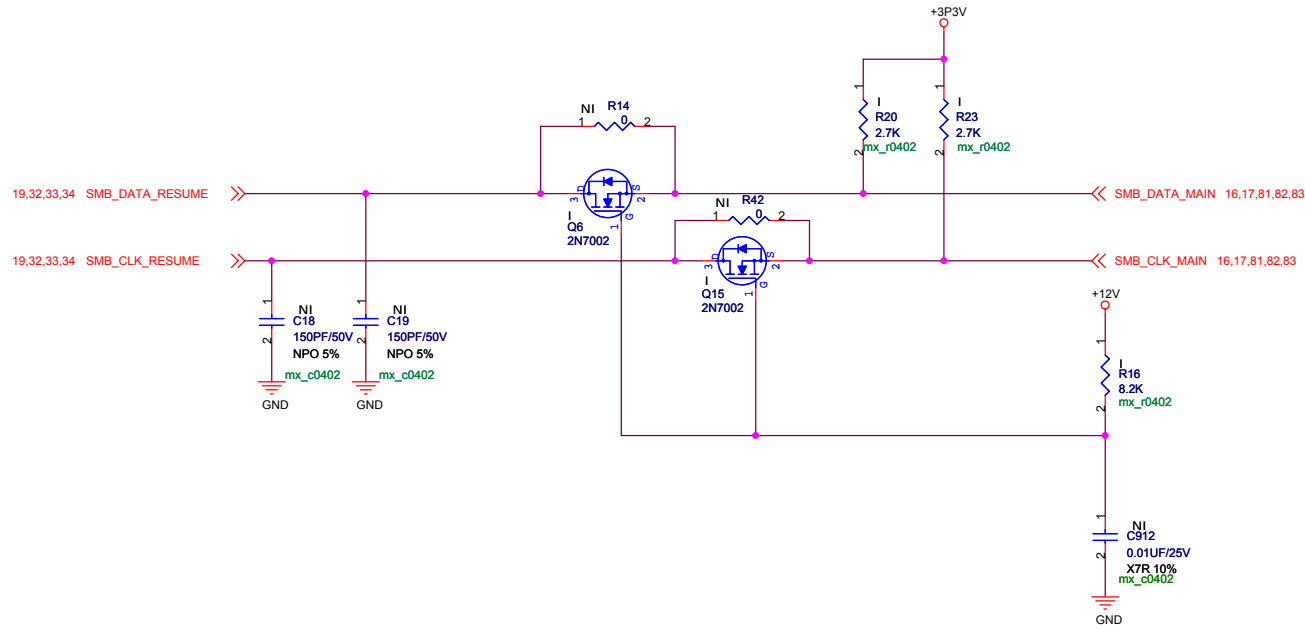
PGD100	PWROK DELEY
0	0 ms
1	100 ms Default

EN_DACOUT	DAC OUTPUT
0	Disable Default
1	Enable

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : SIO W83677 2-2
Size	Project Name	Engineer: Livy_Zhu
A3	IPMSB-BE/CR	
Date: Friday, September 24, 2010	Sheet 53 of 83	Rev 1.00

## SM BUS Control



PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title : SMBUS CONTROL

Pegatron Corp. Engineer: *Livy\_Zhu*

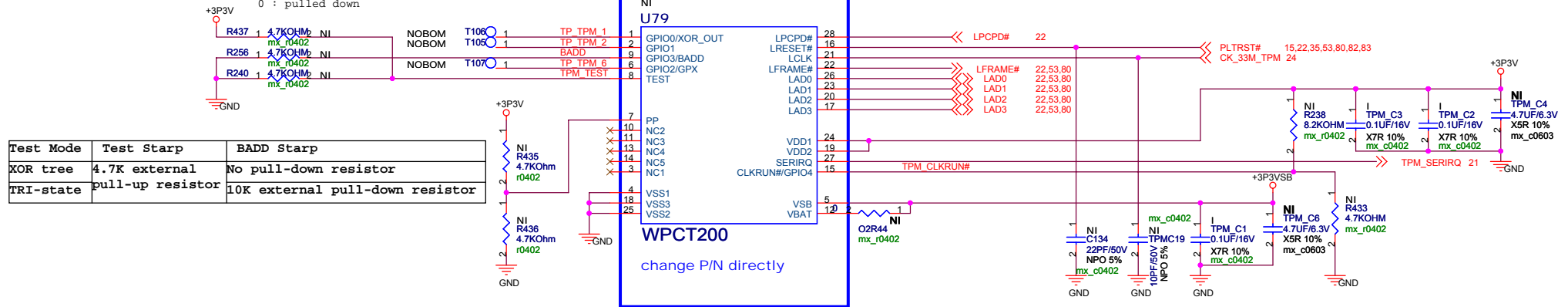
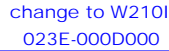
Size A3	Project Name <b>IPMSB-BE/CR</b>	Rev 1.00
------------	------------------------------------	-------------

Date: Friday, September 24, 2010 Sheet 54 of 83

08/13: NI TPM From Fab.B

BADD	SELECTION
0	EEh-EFh
1	7Eh-7Fh

```
1 : left open
0 : pulled down
```



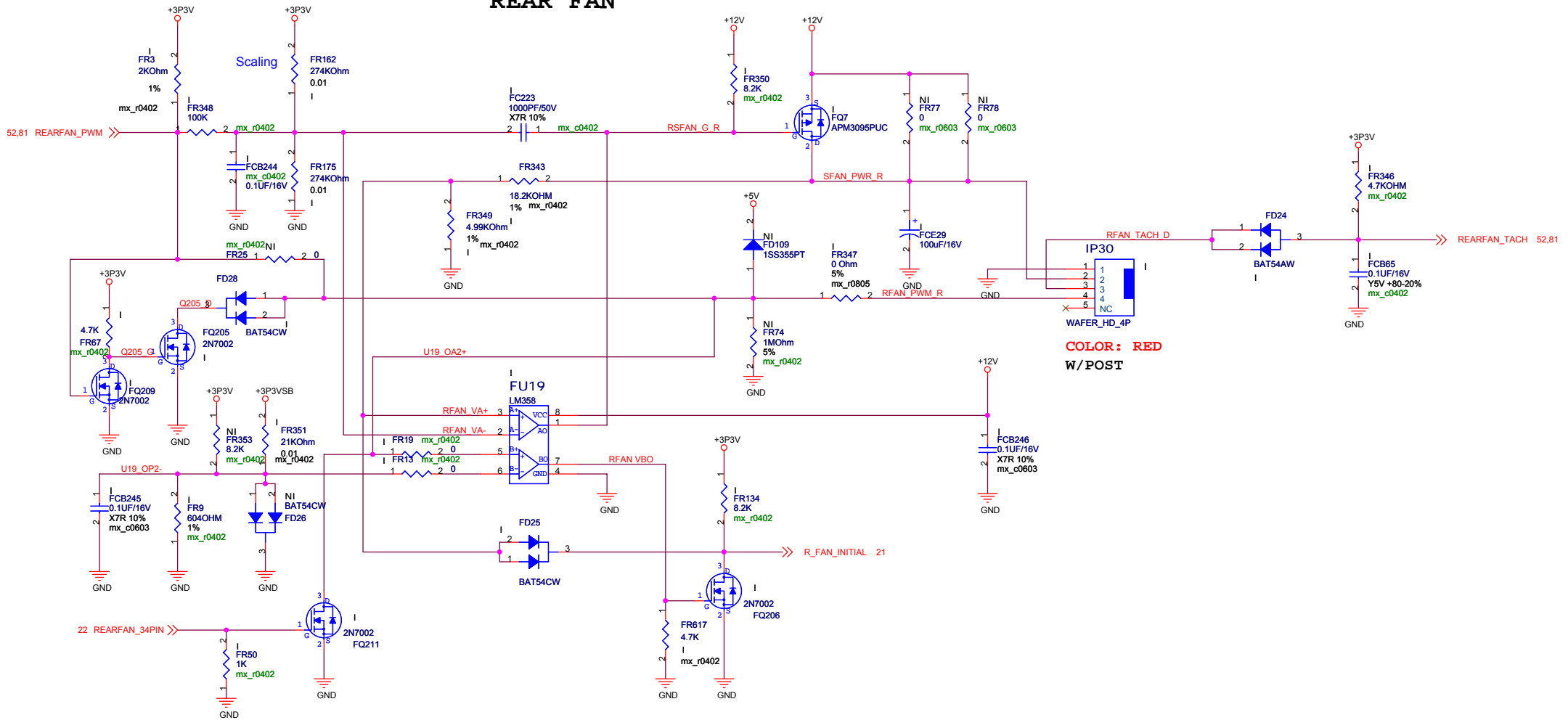
Test Mode	Test Starp	BADD Starp
XOR tree	4.7K external	No pull-down resistor
TRI-state	pull-up resistor	10K external pull-down resistor

W/POST





## REAR FAN

**PEGATRON** Title : REAR FAN CIRCUIT

Size	Project Name	Rev
------	--------------	-----

Date: Friday, September 24, 2010	Sheet 57 of 83
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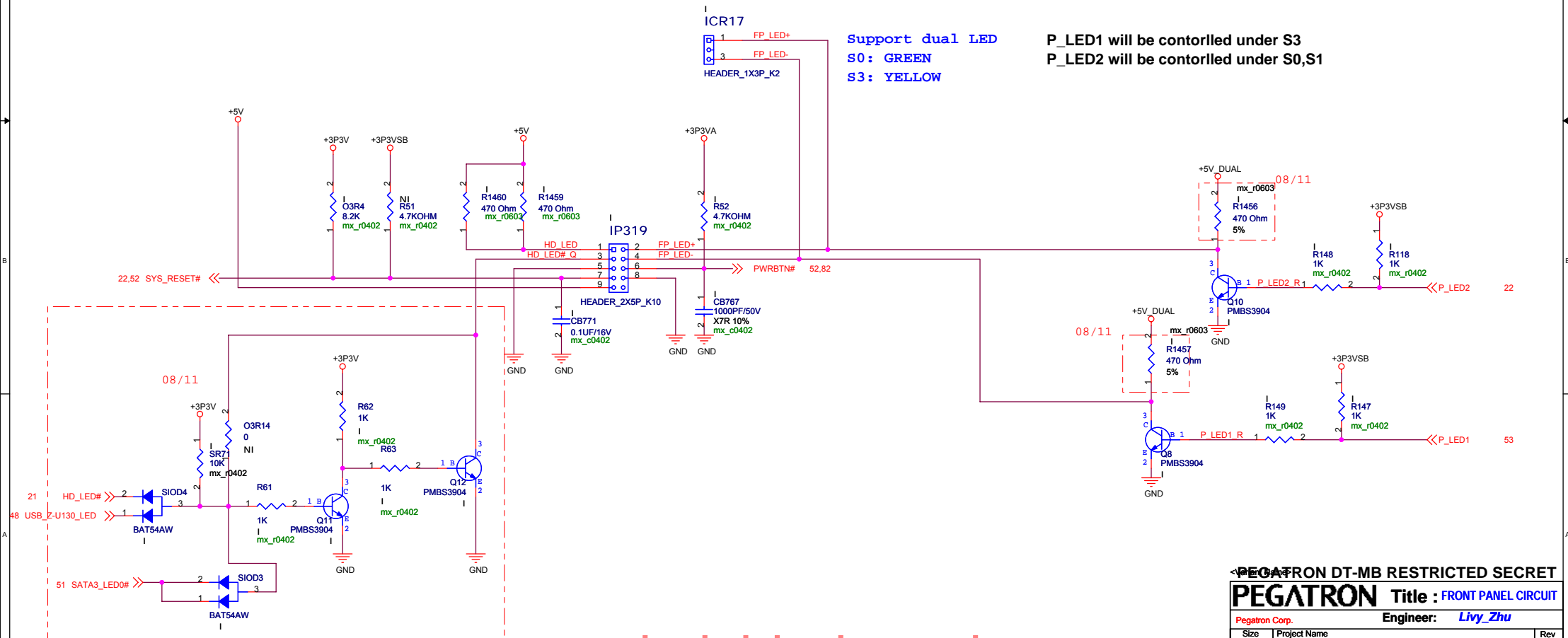
---

# FRONT PANEL / LED CIRCUITRY

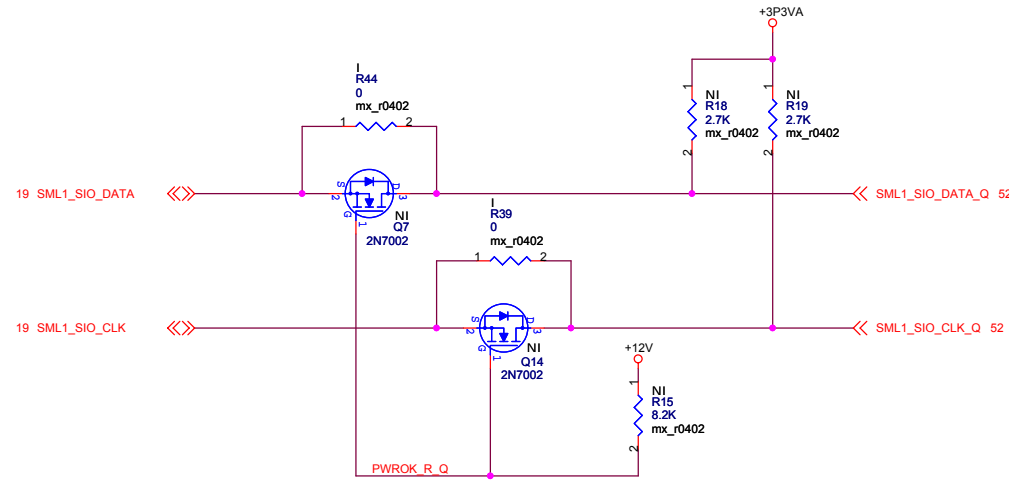
NOTE:  
PWRBTN# of PCH is internally pulled-up in PCH to 3.3 V standby through a weak pull-up 24Kohm.

Support dual LED  
S0: GREEN  
S3: YELLOW

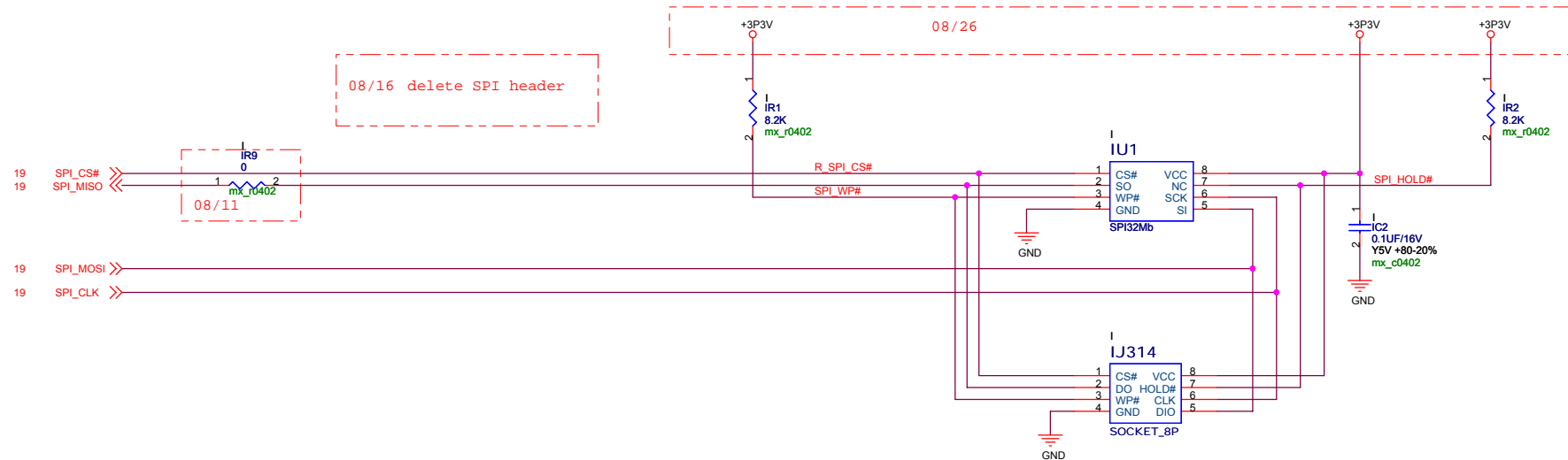
P\_LED1 will be controlled under S3  
P\_LED2 will be controlled under S0,S1



## SM BUS Control



## SPI BIOS ROM - 32 Mbit



PEGATRON DT-MB RESTRICTED SECRET

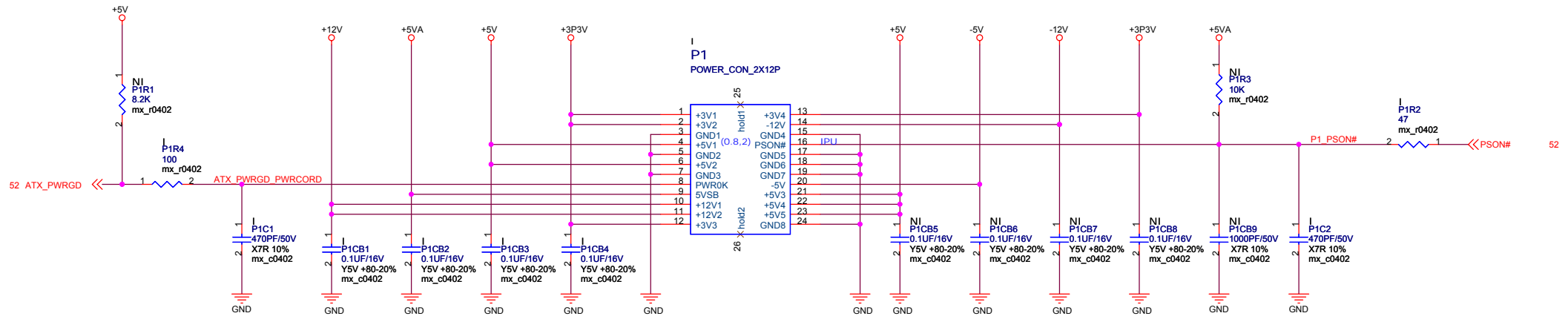
**PEGATRON** Title : SPI ROM

Pegatron Corp. Engineer: Livy\_Zhu

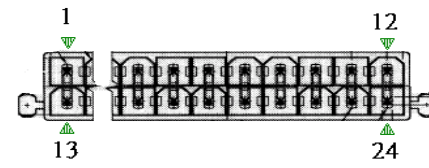
Size A3 Project Name IPMSB-BE/CR

Date: Friday, September 24, 2010 Sheet 59 of 83

## ATX POWER\_24P SUPPLY CONNECTOR

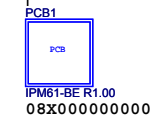


BOTTOM SIDE VIEW

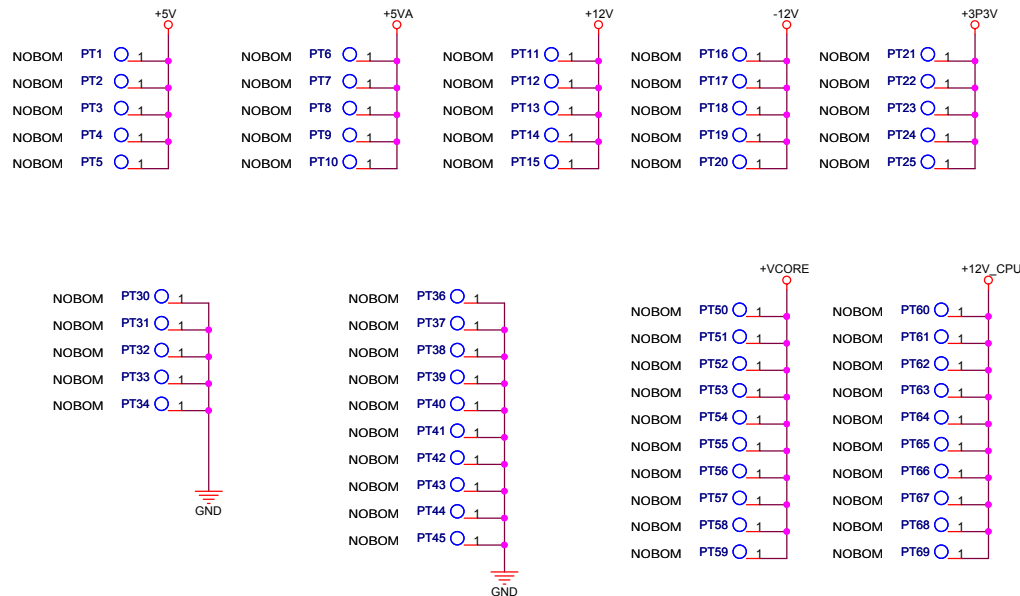


TOP SIDE VIEW

## PCB

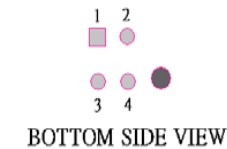
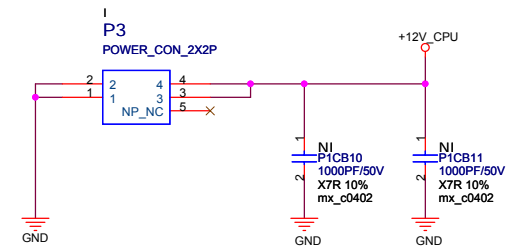


## VRM POWER\_4P SUPPLY CONNECTOR



Nodes related to different power planes

Node	Goal Q'ty
+5V	5
+5VSB	5
+12V	5
-12V	5
+3V	5
+Vcore	10
GND	15
+12V_CPU	10



BOTTOM SIDE VIEW

PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title : ATX 24P CONN

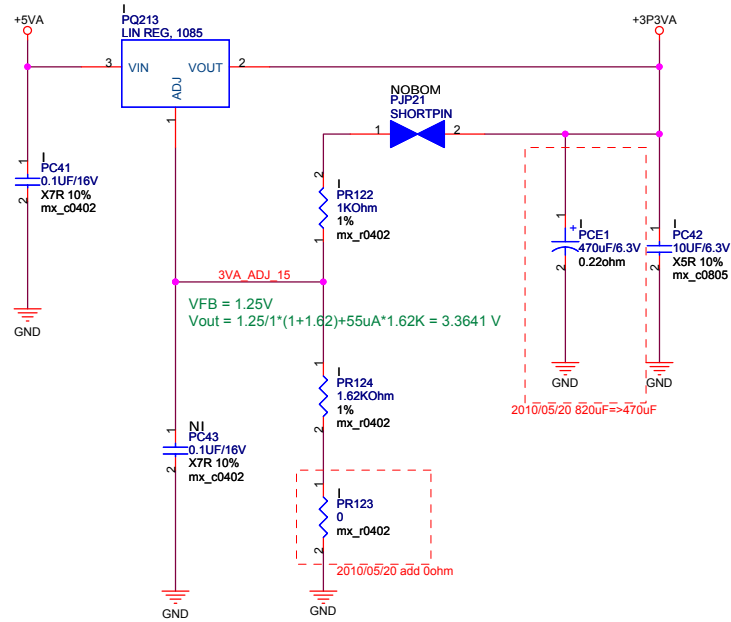
Pegatron Corp. Engineer: *Livy\_Zhu*

Size A3 Project Name IPMSB-BE/CR Rev 1.00

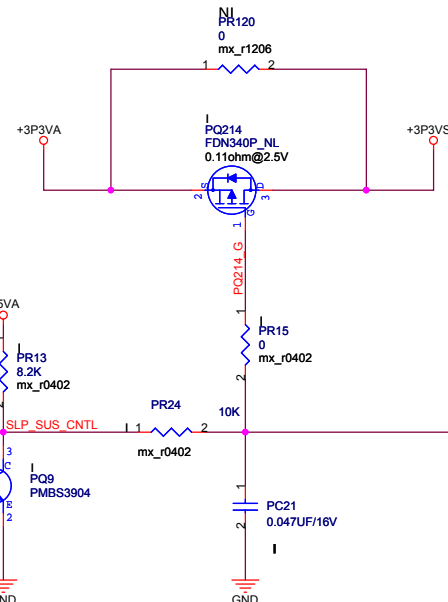
Date: Friday, September 24, 2010 Sheet 60 of 83

# +3P3VA

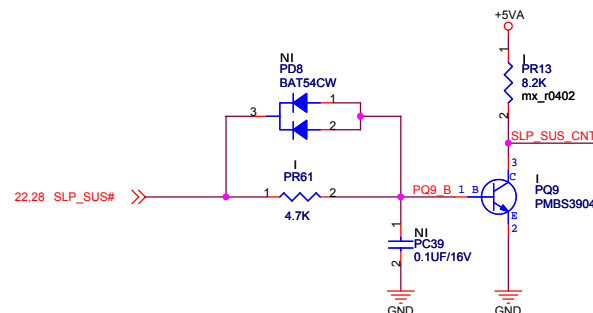
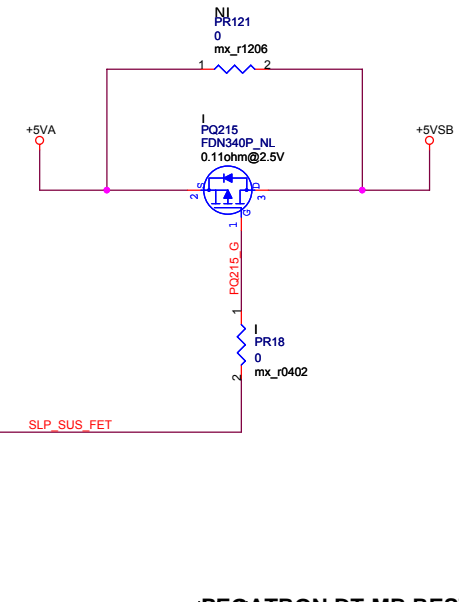
Imax = 1.5A  
Pd = 2.55W



# +3P3VA => +3VSB



# +5VA => +5VSB



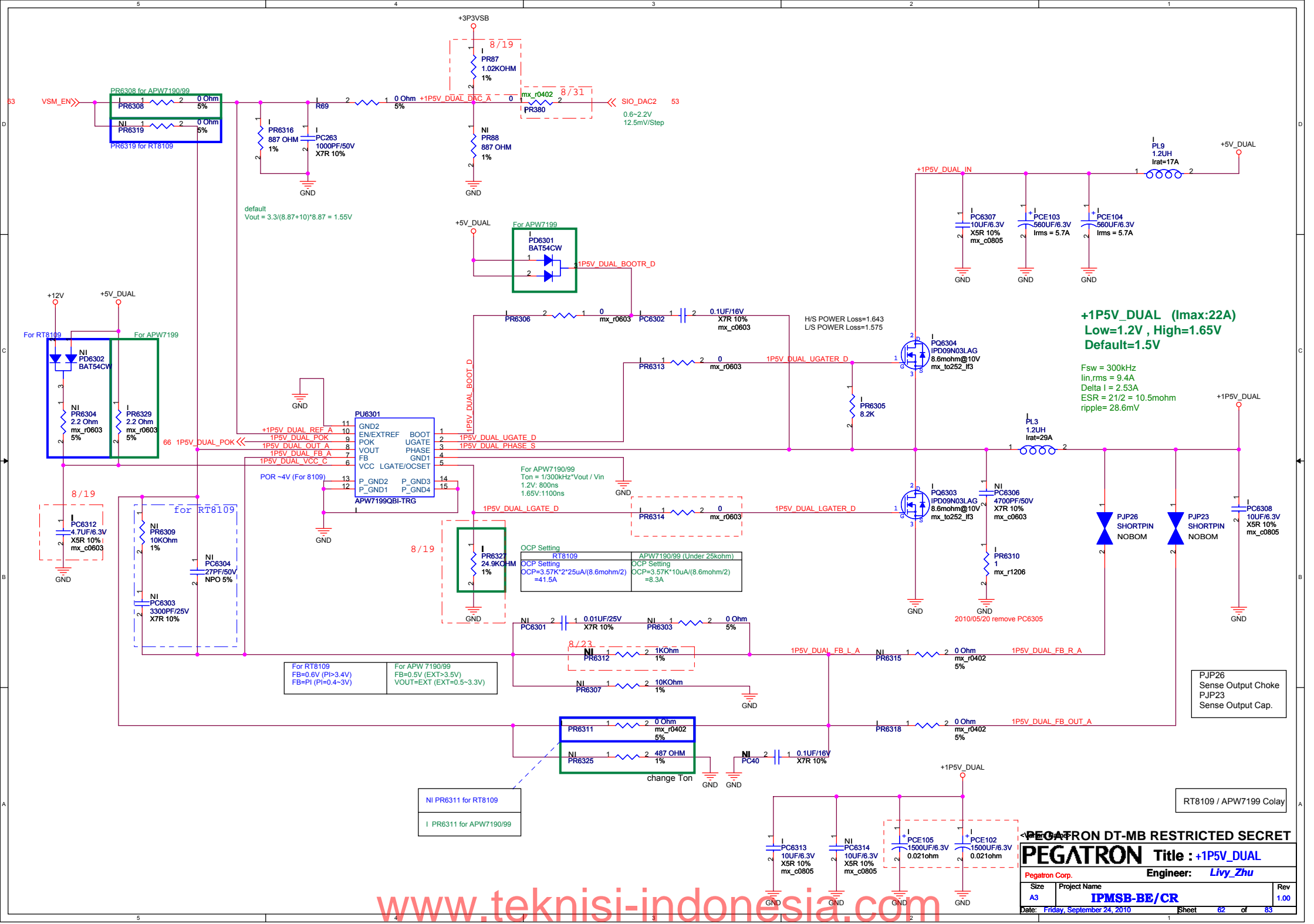
PEGATRON DT-MB RESTRICTED SECRET

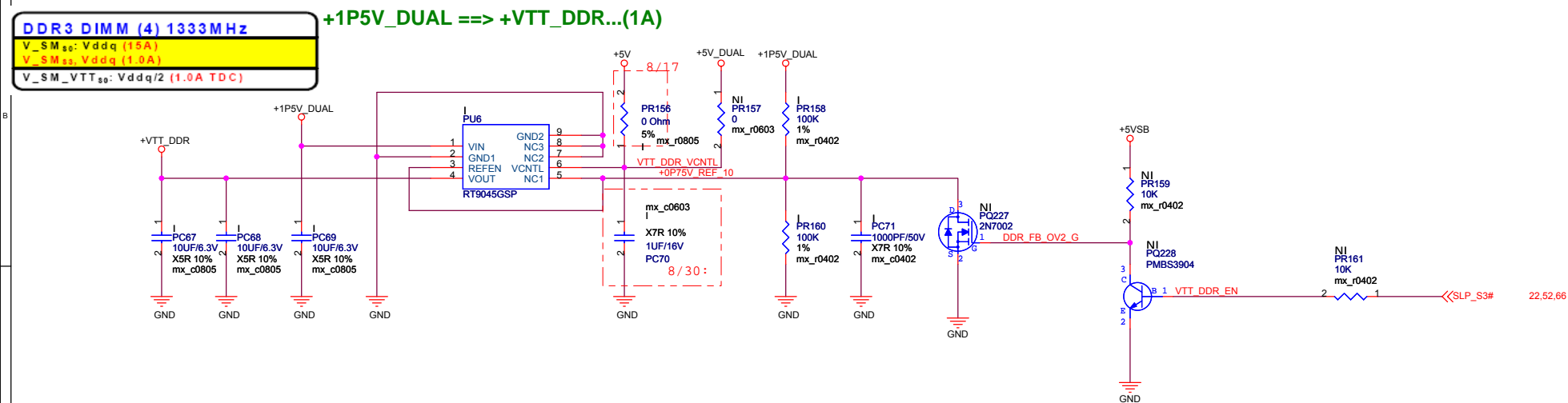
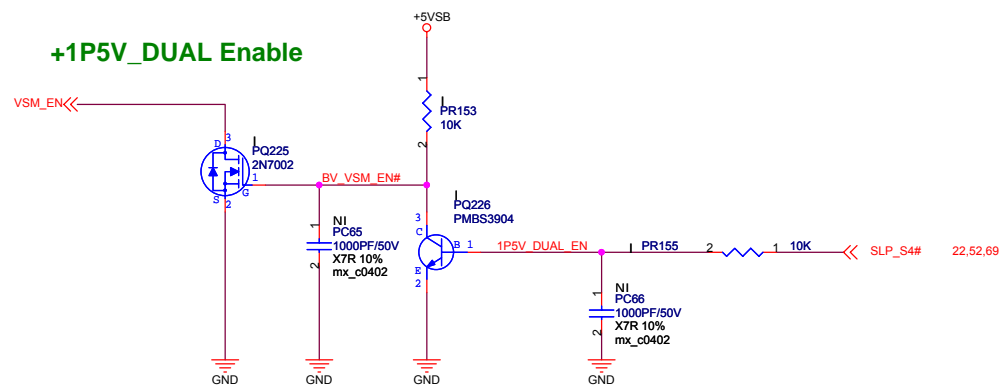
**PEGATRON** Title : +3VA,+3VSB,+5VSB

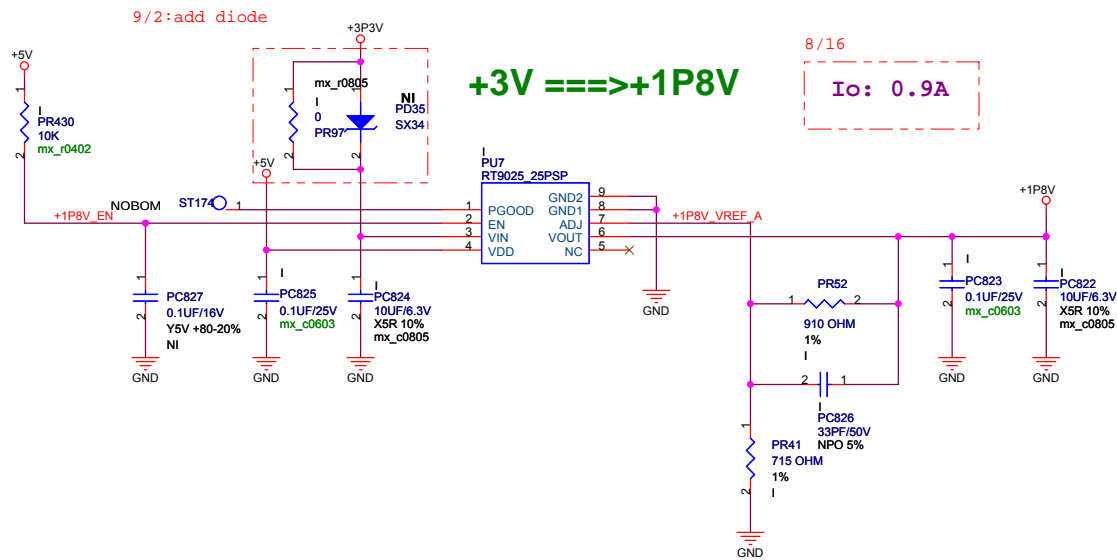
Pegatron Corp. Engineer: *Livy\_Zhu*

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

Date: Friday, September 24, 2010 Sheet 61 of 83

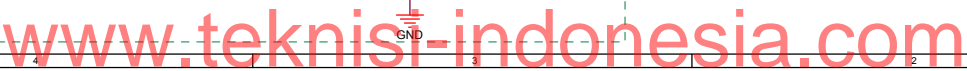








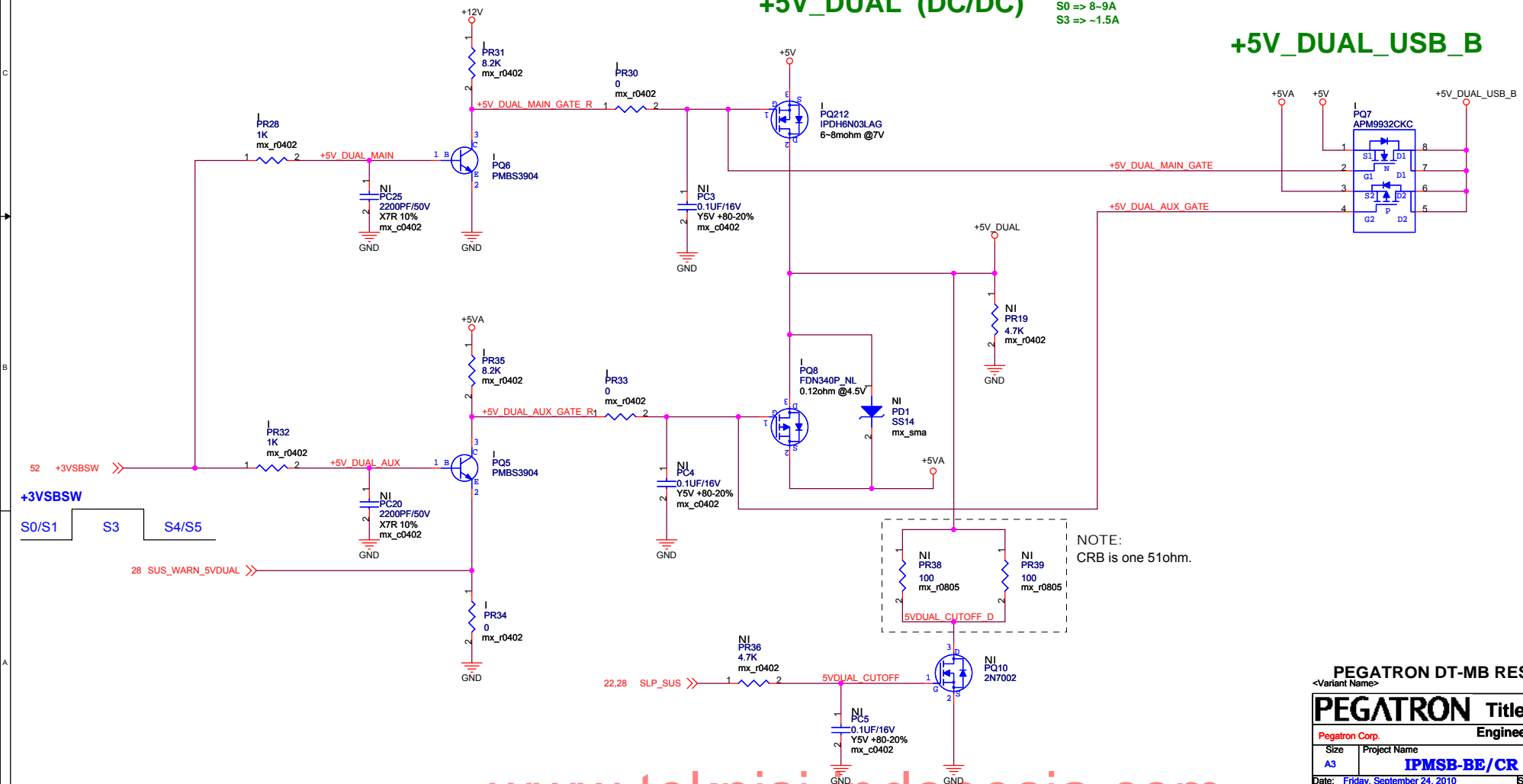




## +5V\_DUAL (DC/DC)

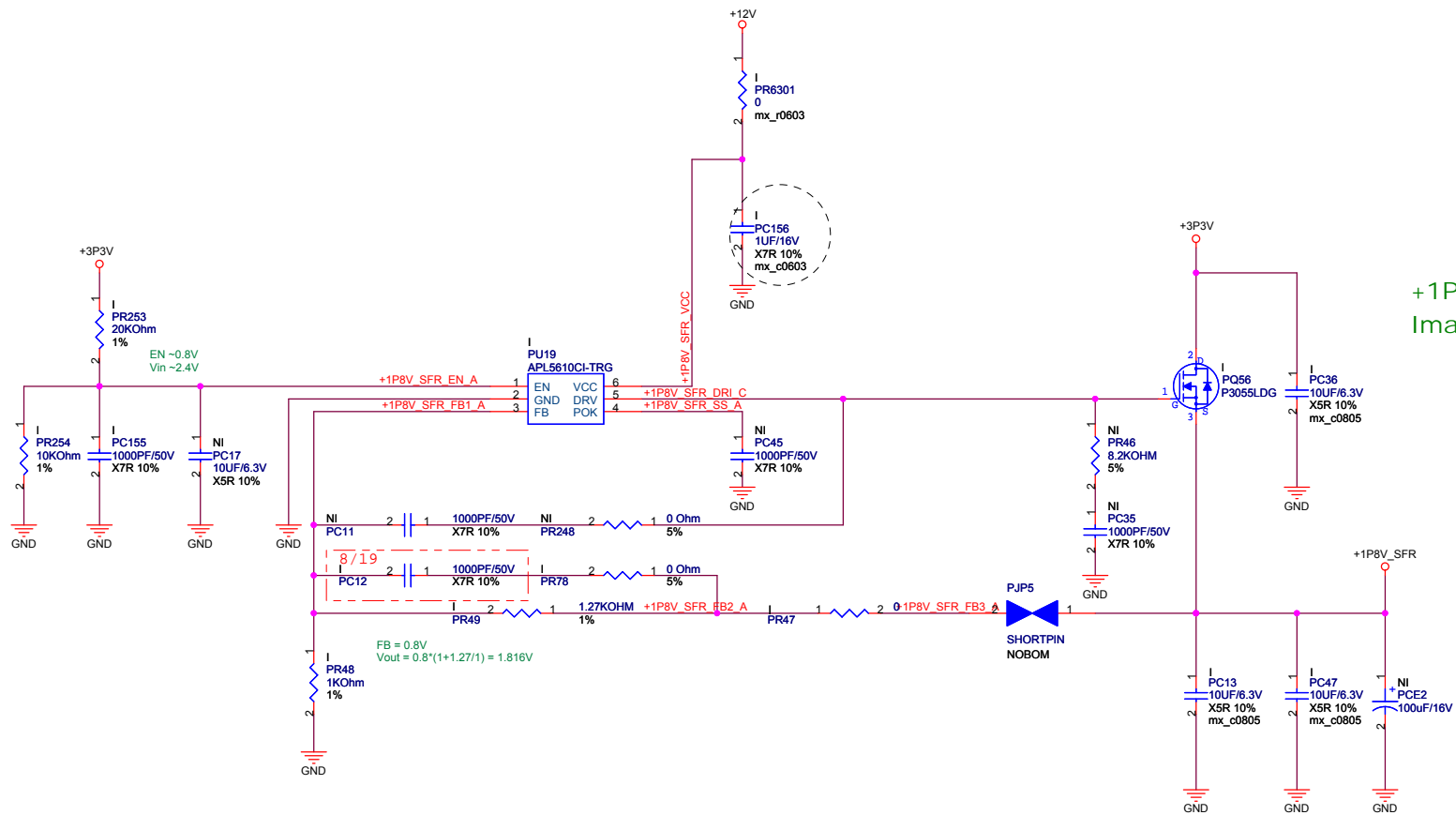
+5V\_DUAL  
S0 => 8-9A  
S3 => -1.5A

## +5V\_DUAL\_USB\_B



PEGATRON DT-MB RESTRICTED SECRET  
<Variant Name>

<b>PEGATRON</b>		Title : <b>DUAL POWER</b>	
Pegatron Corp.		Engineer: <b>Livy_Zhu</b>	
Size A3	Project Name <b>IPMSB-BE/CR</b>	Rev 1.00	
Date: Friday, September 24, 2010		Sheet 67 of 83	



PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title : +1P8V\_SFR

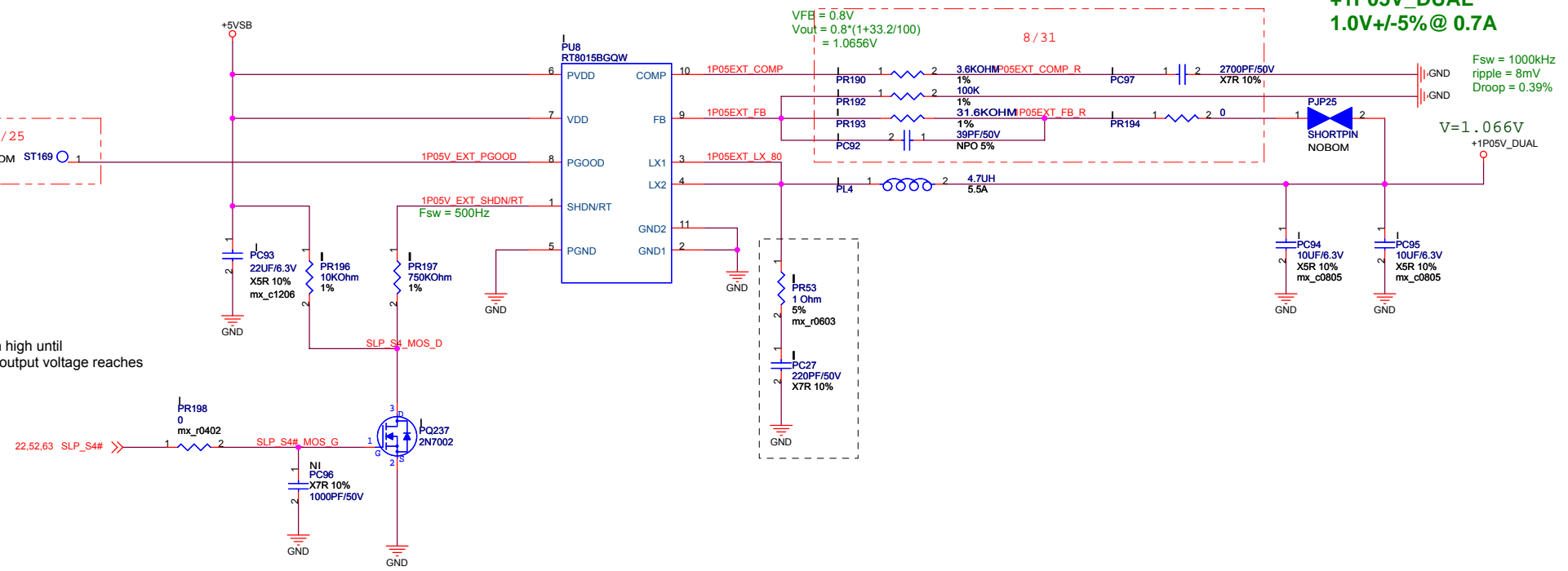
Pegatron Corp. Engineer: Livy\_Zhu

Size A3	Project Name IPMSB-BE/CR	Rev 1.00
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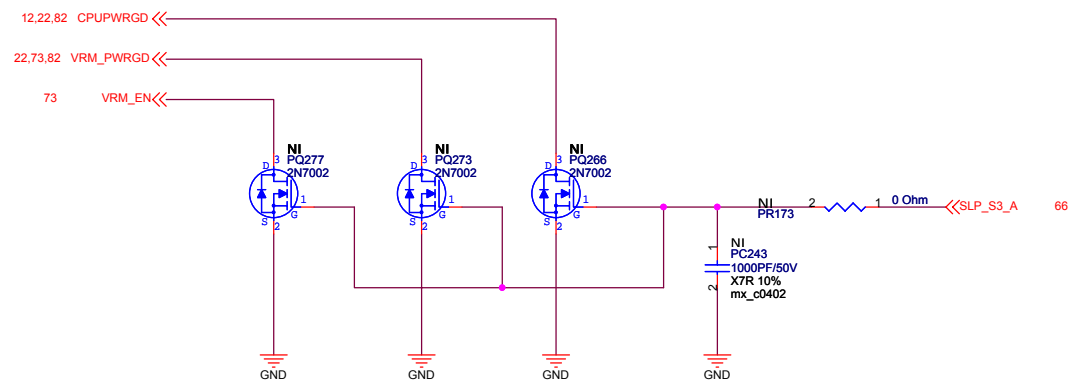
Date: Friday, September 24, 2010 Sheet 68 of 83

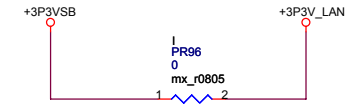
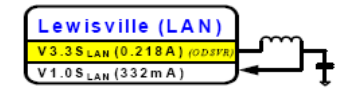
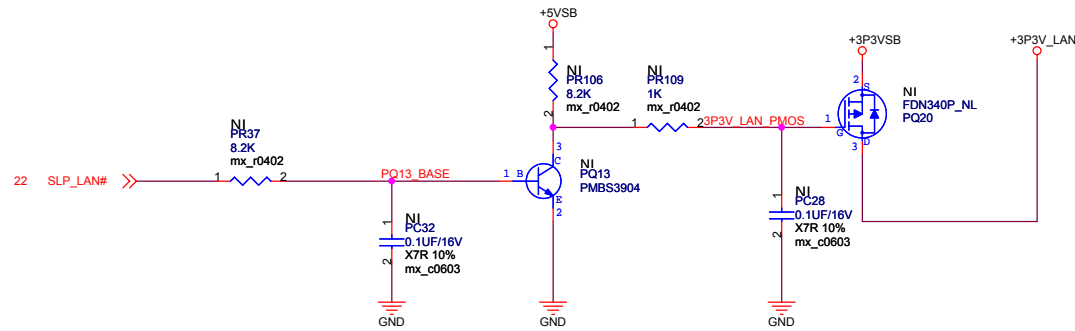
8 / 25  
NOBOM ST169 1

NOTE:  
PGOOD is allowed to transition high until  
soft start finished over and the output voltage reaches  
87.5% of its set voltage.



## VRM\_EN

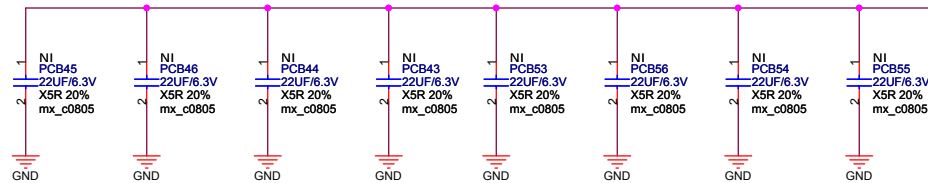
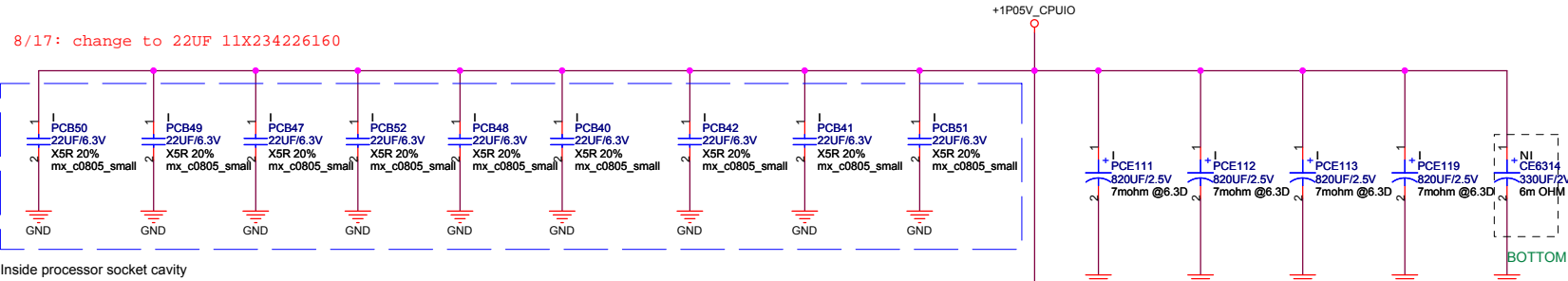
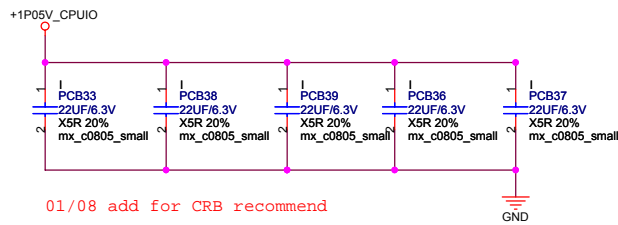




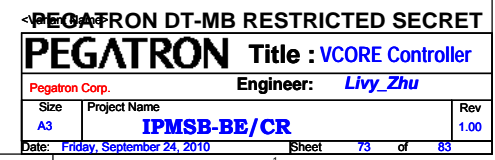
**+3P3V\_LAN**

8/26:delete +3P3V\_ME

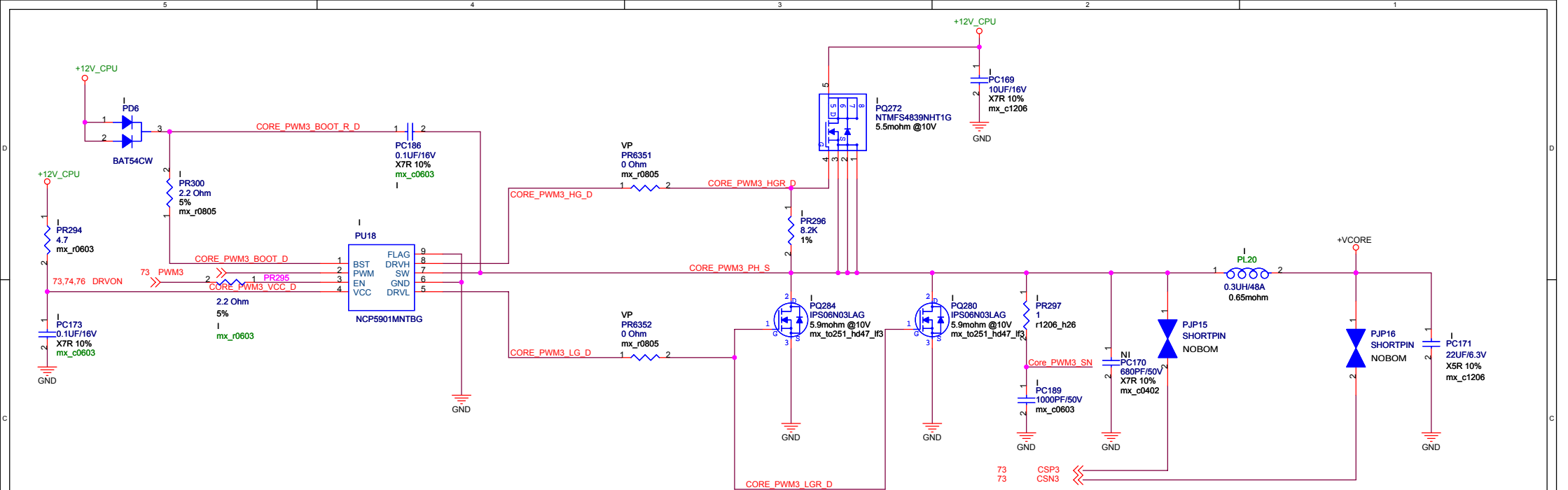






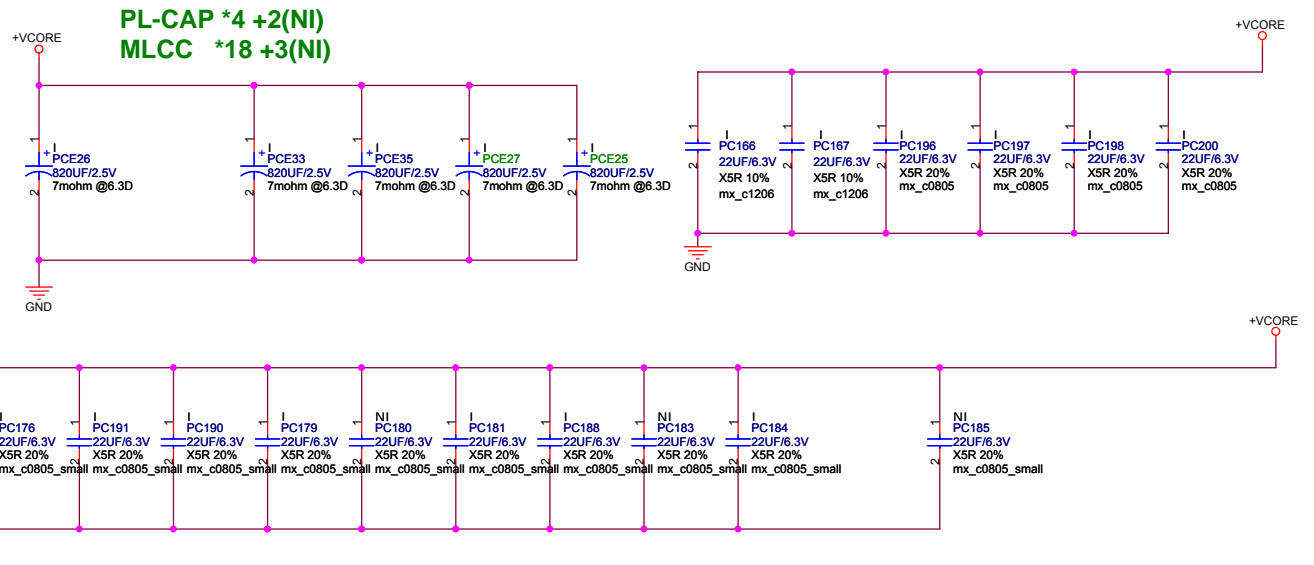






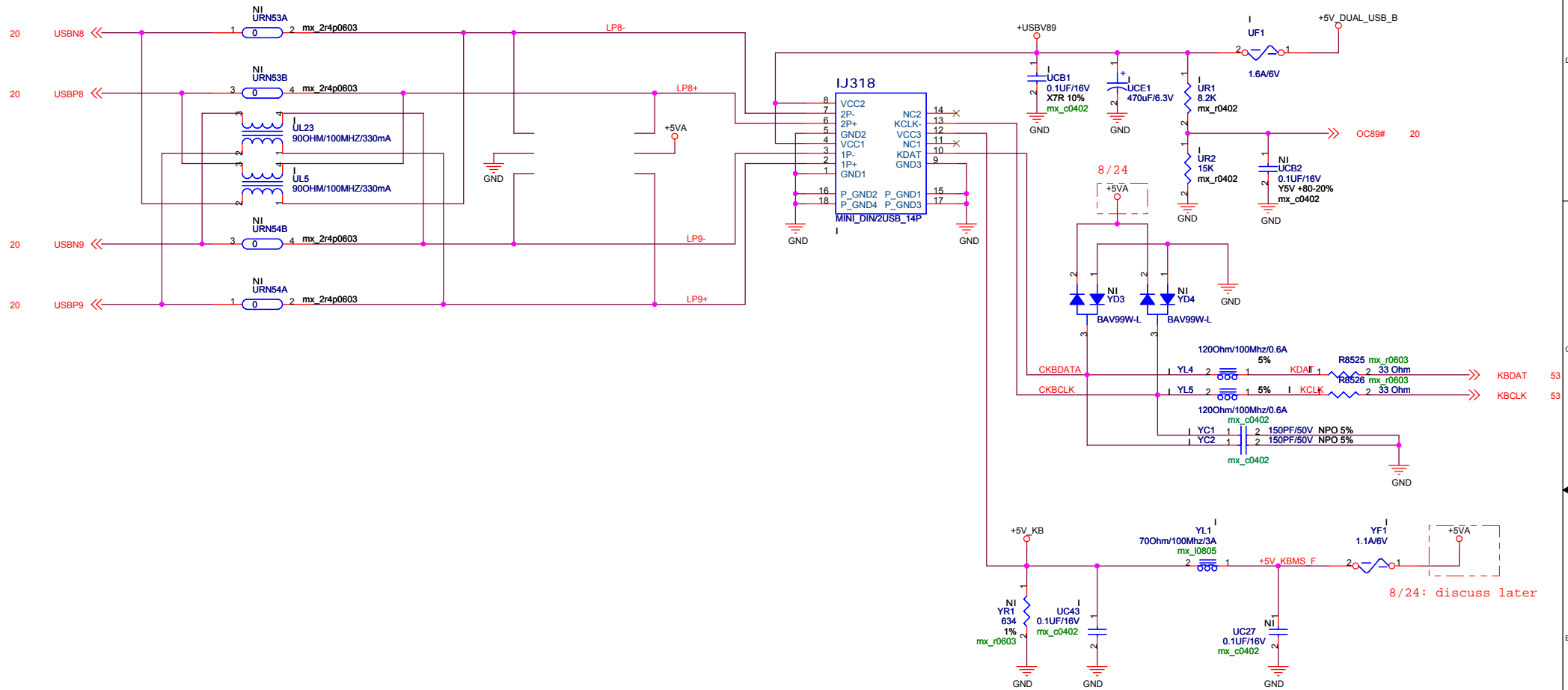
**Output CAP**  
Table 30-2. Decoupling Requirements

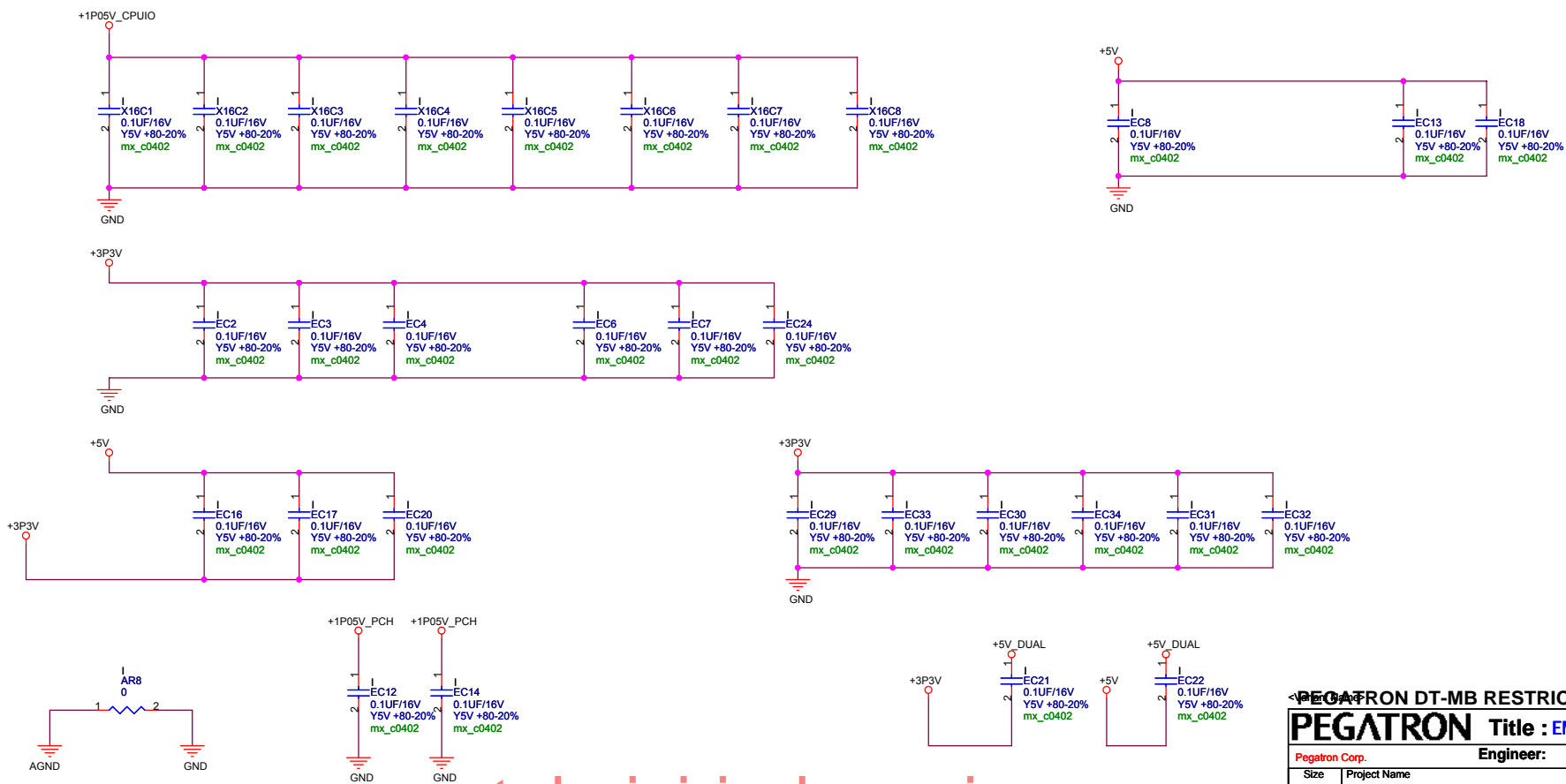
Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560uF	4	7mΩ	1.4nH	Output	North of processor - as close to RM keep-out as possible	1
22uF 0805 X5R	18	5mΩ	0.55nH	Output	14 - Inside processor socket cavity 4- North of processor - as close to RM keep-out as possible	1, 2, 3
Aluminum Electrolytic 390uF	4	51mΩ	6.1nH	Input		1
4.7uF X5R	9	7mΩ	0.6nH	Input		1



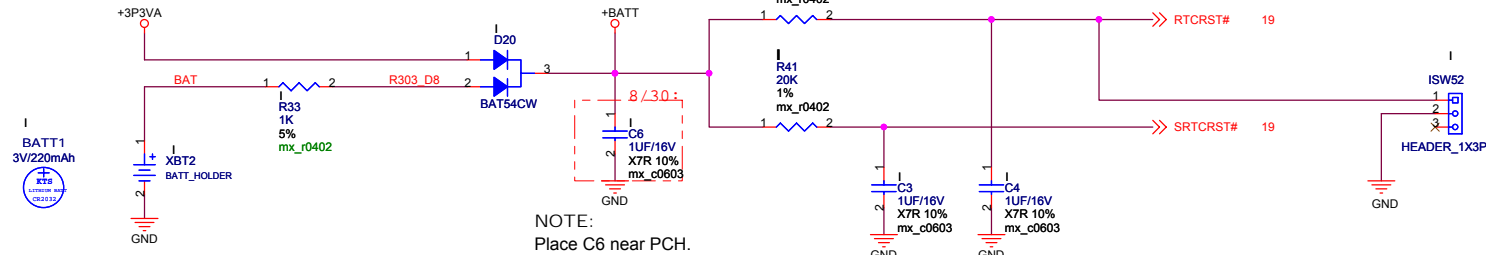


# Back PS/2 with dual USB connector





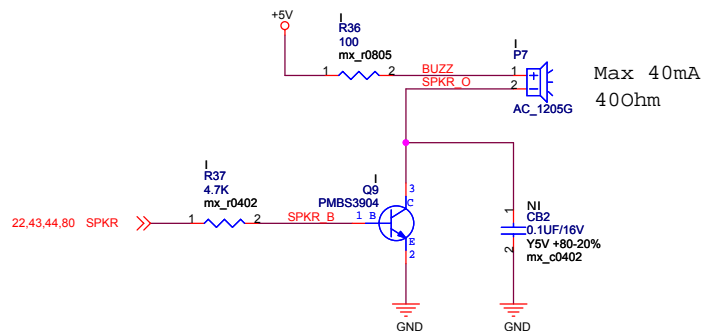
## External RTC Circuitry



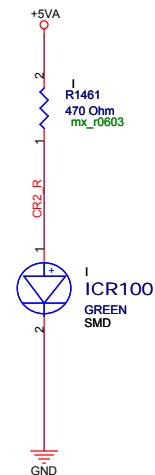
## Battery Socket

## SPEAKER

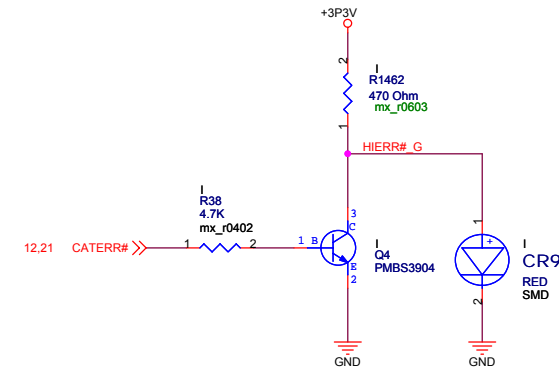
$$I = 5 / (100 + 40) = 35.7 \text{mA}$$



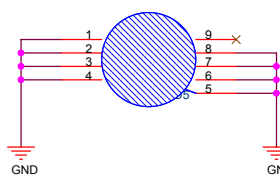
## Standby LED



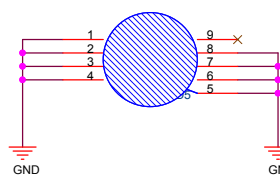
## IERR# : RED



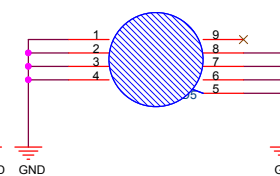
NOBOM  
H1  
SCREW\_HOLE\_160\_HP



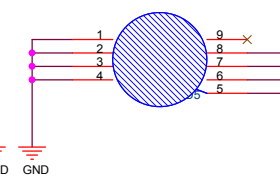
NOBOM  
H3  
SCREW\_HOLE\_160\_HP



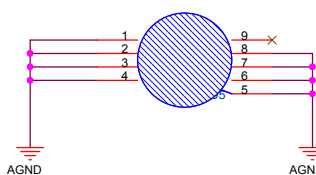
NOBOM  
H4  
SCREW\_HOLE\_160\_HP



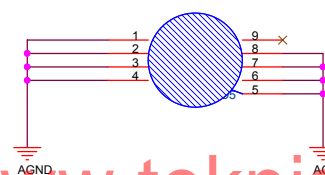
NOBOM  
H5  
SCREW\_HOLE\_160\_HP



NOBOM  
H7  
SCREW\_HOLE\_160\_HP



NOBOM  
H8  
SCREW\_HOLE\_160\_HP



ONLY FOR INTEL SCREW HOLE

LB1  
1.375X0.25  
WHITE  
1D375X0D25\_WHITE

LB2  
1.0X0.187  
WHITE  
1D0X0D187\_WHITE

LB4  
1.0X0.187  
WHITE  
1D0X0D187\_WHITE  
Product code : 1510-06DE0IN

PEGATRON DT-MB RESTRICTED SECRET

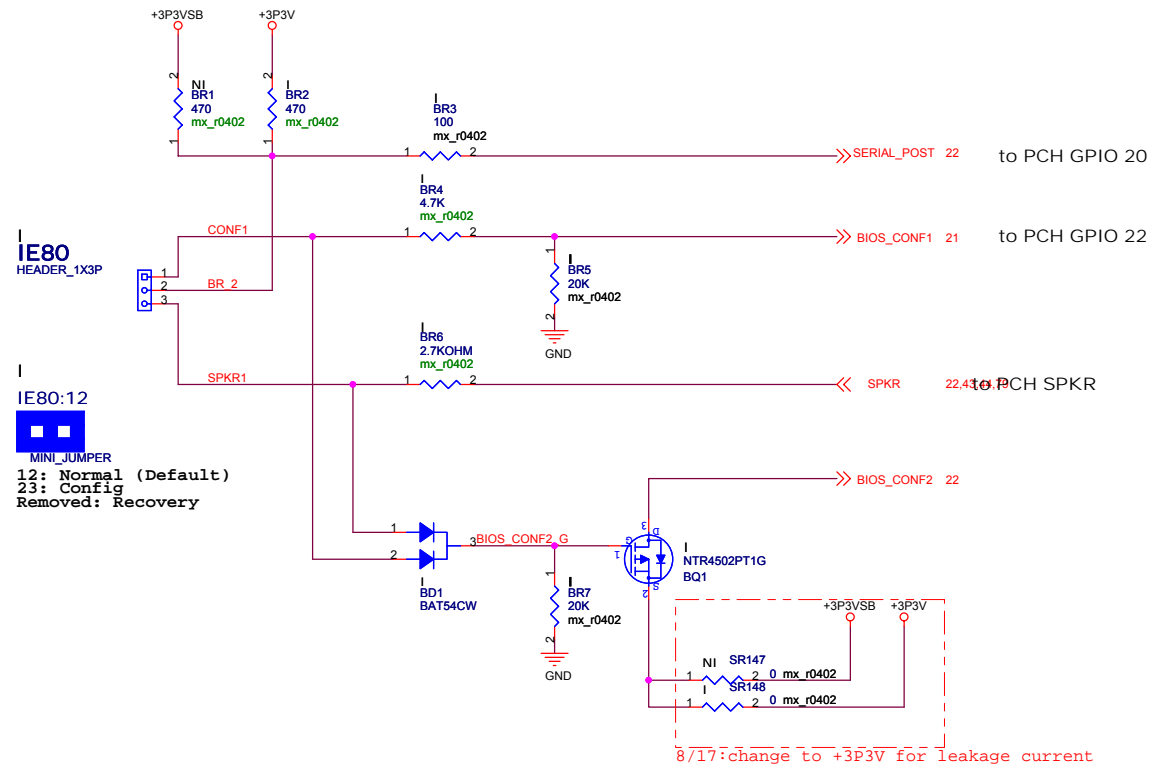
PEGATRON Title : RTC/CMOS/SPKR

Pegatron Corp. Engineer: Livy\_Zhu

Size A3 Project Name IPMSB-BE/CR

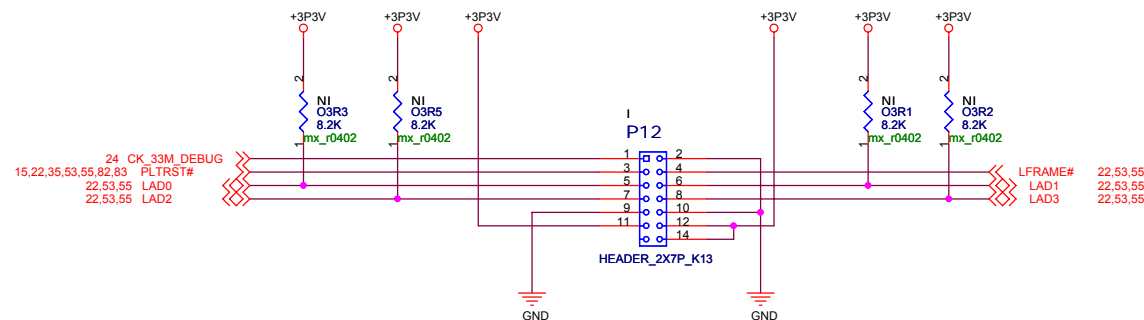
Date: Friday, September 24, 2010 Sheet 79 of 83

## BIOS CONFIGURATION



## LPC DEBUG PORT

08/13: NI LPC From Fab.B  
(after PCI debug verified)



PEGATRON DT-MB RESTRICTED SECRET

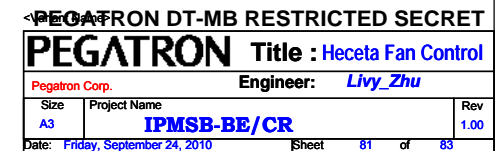
**PEGATRON** Title : BIOS and LPC header

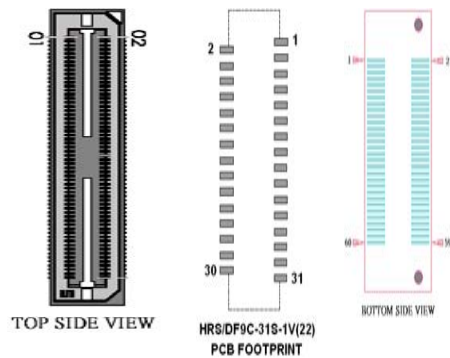
Pegatron Corp. Engineer: *Livy\_Zhu*

Size	Project Name	Rev
A3	IPMSB-BE/CR	1.00

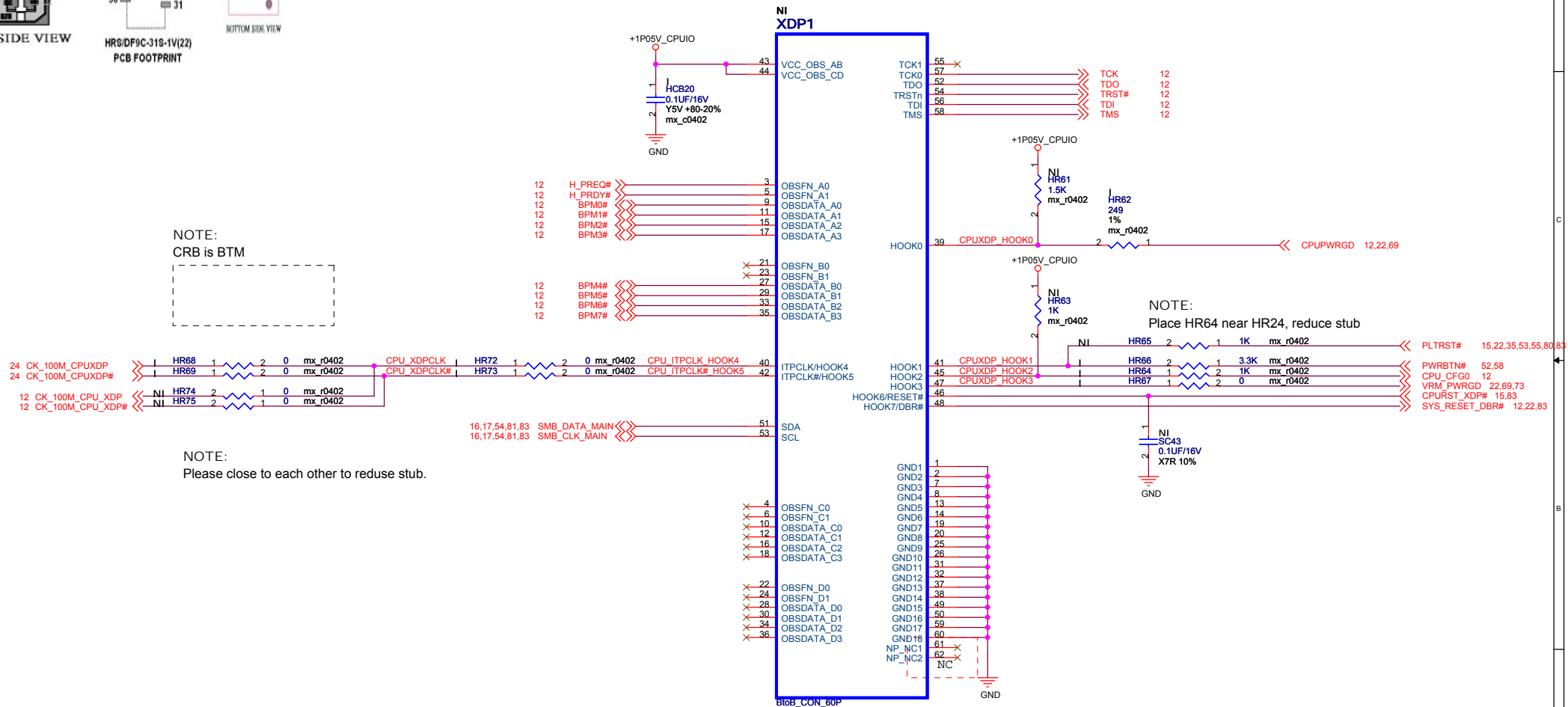
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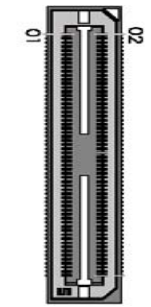




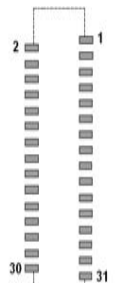


## INTEL CPU XDP DEBUG PORT

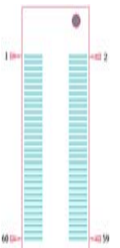




TOP SIDE VIEW



HRS/DF9C-31S-1V(22)  
PCB FOOTPRINT



BOTTOM SIDE VIEW

## INTEL PCH XDP DEBUG PORT

